Exhibit 6

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner,

v.

SOLAS OLED, LTD.,
Patent Owner.

Patent No. 7,446,338

DECLARATION OF ADAM FONTECCHIO, PH.D.

I, Adam Fontecchio, Ph.D., declare as follows:

1. I have been retained as a technical consultant by Samsung Display Co., Ltd., who I have been informed is one of the petitioners in the present proceeding, as well as on behalf of Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc., who I have been informed are identified as "real parties in interest" in the present proceeding. For ease of reference, throughout my declaration, I will refer to these entities collectively as "Samsung" or as the "Petitioner."

2. I have been asked by counsel for the Petitioner to consider whether the references listed as Exhibits 1003-1005 below disclose or suggest, alone or in combination, the limitations recited in the claims of U.S. Patent 7,446,338 (the "'338 patent"). I have also been asked to consider the state of the art and the prior art available before the filing of the '338 patent. I have provided my opinions below.

3. I have been informed that a company known as Solas OLED Ltd. claims to be the owner of the '338 patent. To the best of my knowledge, I have no financial interest in Samsung, Solas OLED Ltd., or the '338 patent. To the best of my recollection, I have had no contact with Solas OLED Ltd. or the named inventors of the '338 patent: Tomoyuki Shirasaki, Tsuyoshi Ozaki, and Jun Ogura. To the extent any mutual funds or other investments that I own have a financial interest in Samsung, Solas OLED Ltd., or the '338 patent, I am not aware of, nor do I have control over, any financial interest that would affect or bias my judgment.

4. I am being compensated at my standard consulting rate for my time, and my compensation is in no way contingent on the results of these or any other proceedings relating to the above-captioned '338 patent.

I. BACKGROUND AND QUALIFICATIONS

5. I am a professor of electrical engineering specializing in electro-optics and displays. I have studied and researched the function and use of numerous types of display technologies, including TFT-LCD, Holographically-formed Polymer Dispersed Liquid Crystal (H-PDLC) displays, Electrophoretic Displays (EPD), nano-Field Emission Displays (nFED), and novel electroluminescent displays including organic light emitting materials. I have conducted extensive research on color filtering, reflective and transmissive displays, and the fundamental interactions of light and matter. I have published numerous articles and delivered many lectures and research talks on these subjects.

6. I have been employed as a faculty member at Drexel University since 2002. Currently, my rank is that of tenured Full Professor. I served as the Vice-Dean of the Graduate College at Drexel University from 2015-2017, and from 2013-2015 served as an Associate Dean of the College of Engineering at Drexel University. Prior to my current position, I was a graduate student at Brown University, working under the direction of Prof. Gregory Crawford, where I conducted doctoral research on new technologies to be used in displays. While

studying at Brown University, I completed a Bachelor's degree in Physics in 1996, a Master's degree in Physics in 1998, and a Doctorate degree in Physics in 2002.

7. During my career as a doctoral student, researcher, and faculty member at Drexel University, I have conducted and directed research that is related, and of interest, to the display community. I have presented my research and findings at professional organizations and conferences including the Society for Information Display, the Optical Society of America, the American Physical Society, the Materials Research Society, and the International Liquid Crystal Society.

8. My research into electro-optic phenomena and devices, as well as my work in engineering education initiatives, has been sponsored by both government agencies and private industry. My government sponsors have included the National Science Foundation, NASA, the Department of Energy, the National Institute of Standards and Technology (NIST), the US Army CERDEC, the Pennsylvania Department of Health, and the Department of Education.

9. I am a Senior Member of the IEEE, have served as Vice-Chair of the IEEE Philadelphia Branch, and am a member of the American Society for Engineering Education (ASEE).

10. I have worked as a consultant on technical issues, including electro-optics and displays, for private clients primarily offering technical guidance, contracted research services, or expert testimony. In the course of my work as a

faculty member and as a consultant, I have visited microfabrication and display fabrication facilities around the world and witnessed the fabrication process first-hand.

11. While a doctoral student at Brown University, I studied the morphology and structure of liquid crystal based devices. Nanoscale microscopy and imaging was a significant part of my thesis work, and I have significant experience with scanning electron microscopy ("SEM"), atomic force microscopy ("AFM"), and surface structure profilometry. For my final two years of graduate school, I served as the in-house expert on SEM, performing the majority of SEM imaging and analysis for the entire research group.

12. At Drexel University, my research has included microfabrication and associated characterization methods, including SEM analysis. I spent several years rebuilding a class 1000 cleanroom with a class 100 wet lab clean room included, which became the shared Micro Fabrication Facility ("MFF"). I also served as Director of Micro/Nano Fabrication, A. J. Drexel Nanotechnology Institute, Drexel University, where I oversaw the acquisition, installation, and operation of microfabrication instrumentation for over 100 users/researchers.

13. In summary, I have extensive familiarity with fields involving displays. Based on my experience, as well as my review of the literature, I am familiar with

what the state of this field was at the relevant time up to the time that the ’338 patent was filed.

14. In addition to my education and work experience that I have outlined above, a complete list of my work experience, awards, honors, and publications that may be relevant to the opinions are set forth in my CV (Exhibit 1019).

II. MATERIALS CONSIDERED

15. I am not an attorney and I am not offering any legal opinions as part of this declaration. However, through my consulting work I have had experience studying and analyzing patents and patent claims from the perspective of a person of ordinary skill in the art.

16. I have reviewed the ’338 patent—both its claims and its specification—as well as the associated file history for the application that led to the ’338 patent. In addition, I have reviewed a number of prior art references. I have provided below a complete list of materials considered in rendering the opinions found in this declaration:

Exhibit	Description
1001	U.S. Patent No. 7,446,338 (the “’338 patent”)
1002	File History for U.S. Patent No. 7,446,338
1003	U.S. Patent Application Pub. No. 2002/0158835 (“Kobayashi”)
1004	U.S. Patent Application Pub. No. 2004/0113873 (“Shirasaki”)

Exhibit	Description
1005	International Publication No. WO 03/079441 ("Childs")
1006	European Patent Application No. EP 1331666 ("Yamazaki")
1007	U.S. Patent Application Pub. No. 2004/0165003 ("Shirasaki II")
1008	Japanese Patent Publication No. 2004-258172
1009	U.S. Patent Application Pub. No. 2003/0151637 ("Nakamura")
1010	International Publication No. WO 03/079442 ("Hector")
1011	International Publication No. WO 03/079449 ("Young")
1012	Tsujimura, Takatoshi. *OLED Display Fundamentals and Applications: Fundamentals and Applications*, John Wiley & Sons, Incorporated, 2012 ("Tsujimura")
1013	Crawford, Gregory P. *Flexible flat panel display technology*. Vol. 3. West Sussex: Wiley, 2005 ("Crawford")
1014	U.S. Patent Application Pub. No. 2003/0127657 ("Park")
1015	U.S. Patent No. 7,498,733 ("Shimoda")
1016	U.S. Patent Application Pub. No. 2002/0000576 ("Inukai")
1017	U.S. Patent Application Pub. No. 2002/0009538 ("Arai")

III. RELEVANT LEGAL STANDARDS

17. As I noted earlier, I am not an attorney and do not provide any legal opinions as part of this declaration. However, for the purposes of this declaration, I have been informed about certain aspects of the law by the attorneys for Petitioner that are relevant to forming my opinions. Below is a summary of the law that has been explained and provided to me.

a. Anticipation

18. Petitioner's counsel has informed me that a patent claim may be "anticipated" if each element of that claim is present either explicitly or inherently in a single prior art reference, and that the elements should be arranged in the reference as in the claim. Petitioner's counsel has informed me that for a claimed limitation to be inherently present, the prior art need not expressly disclose the limitation, so long as the claimed limitation necessarily flows from a disclosure in the prior art.

b. Obviousness

19. Petitioner's counsel has informed me that even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

20. Petitioner's counsel has informed me that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

a) the level of ordinary skill in the art at the time the application was filed;

b) the scope and content of the prior art; and

c) what differences, if any, existed between the claimed invention and the prior art.

21. Petitioner's counsel has informed me that a single reference can render a patent claim obvious by itself if any differences between that reference and the claims would have been obvious to a person of ordinary skill in the art. Alternatively, the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

a) whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results;

b) whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent;

c) whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

d) whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;

e) whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so; and

f) whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art.

22. Petitioner's counsel has informed me that one of ordinary skill in the art has ordinary creativity and is not an automaton. Petitioner's counsel has informed me that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

23. Petitioner's counsel has informed me that under specific circumstances whereby a secondary reference is not being used to teach a limitation but rather to explain the teachings of a primary reference, a specific motivation to combine need not be identified; however, in the case of the combination of art discussed in this declaration, a specific motivation to combine is present and I have identified it.

24. Petitioner's counsel has also informed me that, in this proceeding, the claim terms should be given their plain and ordinary meaning as understood by a person of ordinary skill in the art ("POSA"), consistent with the disclosure and the prosecution history.

IV. TECHNOLOGICAL BACKGROUND

25. According to the face of the ’338 patent, the ’338 patent was filed in the United States on September 26, 2005. Ex. 1001 at cover. However, the ’338 patent claims priority to a Japanese patent application (2004-283824), which the ’338 patent states was filed on September 29, 2004. Ex. 1001 at cover. Accordingly, for purposes of my discussion below, I assume that the timeframe of the purported invention of the ’338 patent was September 2004, and have provided an overview of the technological background of active matrix OLED matrix displays by this September 2004 timeframe. In particular, I have provided a discussion of the state of the art of active matrix OLED technology in September 2004, particularly as relates to the technology described in the ’338 patent.

a. Passive vs. Active Matrix OLED Displays

26. Passive matrix addressing is a convenient method of addressing a large array of pixels when using a top to bottom electrode system. This particular method works through orthogonal rows and columns of individually electrically controlled electrodes located on the top and bottom of the switchable sample. By activating a row on the top and a column on the bottom, only in the intersection of the row and column is there a large enough electric field to completely activate the pixel. Historically, the passive matrix system was employed primarily for large arrays where running a trace to each pixel is space prohibitive. Passive addressing has some

significant limitations, such as the inability to create a ring structure, or a structure with a cutout in the center.

27. Active matrix addressing was designed in an effort to overcome the issues encountered in multiplexing devices like passive matrix displays, by way of adding individual modulation of each pixel using a pixel-by-pixel switch. The dominant technology used in active matrix addressing is thin film transistor ("TFT") technology. Originally demonstrated as a potential driving element in 1966 by RCA, transistors act as individual on-off switches at each pixel.

28. In an active matrix display, each individual pixel contains at least one thin film transistor and a storage capacitor. Rows and columns of the display are then used to control the transistors, which in turn modulate the current across the organic emission layer.

29. Row and column drivers are generally attached to the edges of the TFT array glass substrate to supply the address and data signals to the pixels. The row and column drivers receive their signals from one or more controller circuits mounted on a printed circuit board.

30. Given the superior picture quality, speed, and driving voltages, active matrix technology is the primary driving method in use today for displays. Since the late 1990s and early 2000s, active matrix technology has taken over from passive

matrix displays, and it is unusual to find passive matrix drive methods in any significant display technology today.

31. Active matrix technology has been used with multiple types of flat panel displays, including liquid crystal displays (LCDs), as well as the organic electroluminescent displays described in the ’338 patent and the prior art.

32. In organic electroluminescent displays, which make use of organic light emitting diodes (OLEDs), a voltage is applied to one or more layers of organic semiconductor material(s), which will emit light of various wavelengths, based on the composition of the layer(s). Active matrix OLED display technology is commonly referred to as “AMOLED.”

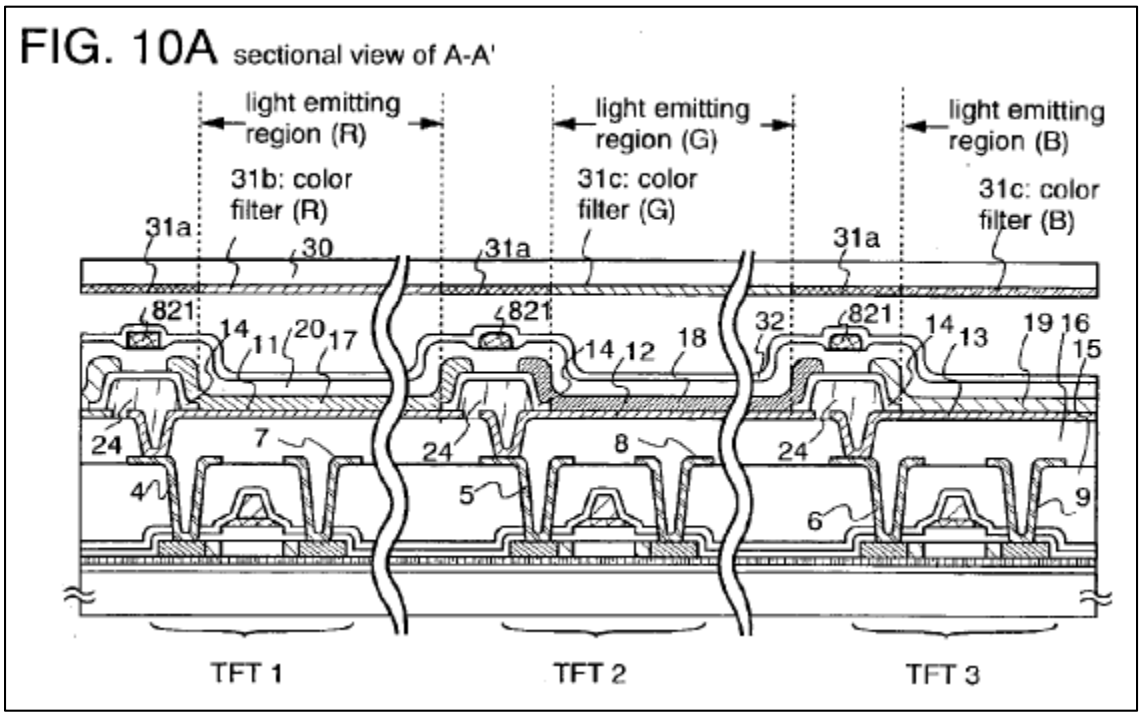
b. Lowering Resistance of Components in an AMOLED Display

33. As I have discussed above, AMOLED displays were widely known by the September 2004 timeframe of the ’338 patent. One well-known issue presented by such AMOLED displays, however, was the potential for what is known as “voltage drop” across the relatively thin conductive components of an AMOLED display. “Voltage drop” refers to the decrease in electrical potential along the path of a current flowing through a conductive element, due to the internal resistance of the conductive element itself. This internal resistance to electron flow is due to the properties of the material itself, and is a fundamental characteristic known as “resistivity.”

34. Because the conductive elements of an AMOLED display (such as the lines that carry a supply current and/or a signal current, or the electrodes of the OLED elements in each pixel) are each relatively thin, they have a relatively high resistance (a conductive element with a smaller cross-section will have a higher resistance than a conductive element made from the same material but with a larger cross-section). Accordingly, because of the high resistance of each of these conductive elements, the energy supplied to these conductive elements will dissipate along their length, resulting in a disparity between the power available at the beginning of the conductive element as compared to the power available at its end.

35. To remedy this issue, it was well known by the September 2004 timeframe of the '338 patent to supplement and/or replace conductive elements in an AMOLED structure with added or "auxiliary" low-resistance conductive material (often of larger cross-section than the original conductive element) that would bring down the resistance of those conductive elements. For example, European Patent Application No. EP 1331666 to Yamazaki et al. ("Yamazaki") (Ex. 1006) explains that at least one of the anode or cathode of the OLED pixel element is made out of a "transparent conductive film (typically ITO or ZnO)," Ex. 1006 at ¶ [0029], but that these materials have a "relatively high resistance value" and thus cannot transmit power uniformly, making it "difficult to achieve a large screen," Ex. 1006 at ¶ [0059].

36. To solve this problem, Yamazaki discloses electrically connecting lower-resistance "auxiliary electrodes" to the transparent pixel electrode, which "function to decrease an electric resistance value" of the pixel electrode and allow "the thickness of the transparent conductive film [to] be reduced" even further. Ex. 1006 at ¶ [0059]. Yamazaki provides several examples of such "auxiliary electrodes" (which can be formed of a number of different metals, including aluminum and copper, Ex. 1006 at ¶ [0060]), such as "auxiliary electrodes 821" formed on transparent cathode 20 so that "the cathode . . . can be decreased in resistance in its entirety" and "can be made thin," Ex. 1006 at ¶ [0106], as illustrated by Fig. 10A of Yamazaki:



37. Other contemporary prior art similarly described such auxiliary conductive elements. International Publication No. WO 03/079442 ("Hector") (Ex. 1010) described such "auxiliary wiring for reducing the resistance of (and hence the voltage drops across) the common upper electrode of the electroluminescent elements," Ex. 1010 at 1:30-2:2, as did International Publication No. WO 03/079449 ("Young") (Ex. 1011), Ex. 1011 at 2:3-7.

38. Further, in addition to auxiliary electrodes that decrease the resistance of OLED electrodes, both Hector and Young also described supplemental "interconnections" designed to decrease the resistance of other conductive lines in the OLED structure. Hector, for example, explained that the thin-film transistor array of the AMOLED device is connected to various "voltage supply lines," but that "[v]oltage drops along these two supply lines can result in incorrect drive currents for individual pixels. This can lead to a decrease in emission intensity (i.e. fading of the image) from pixels in the center of the display. Indeed, with large-area displays, the effect may be so bad that no emission occurs at the center, so limiting the acceptable display size." Ex. 1010 at 2:3-16. To solve this problem, Hector proposed electrically connecting the supply lines to thick "conductive barrier material," which causes "the electrical resistance along the drive supply line (and consequential voltage drops)" to "be significantly reduced" and "the image quality

[to] be improved." Ex. 1010 at 3:1-23. Such "conductive barriers" are illustrated, for example, by elements 240 in Fig. 1 of Hector, Ex. 1010 at 10:24-32:

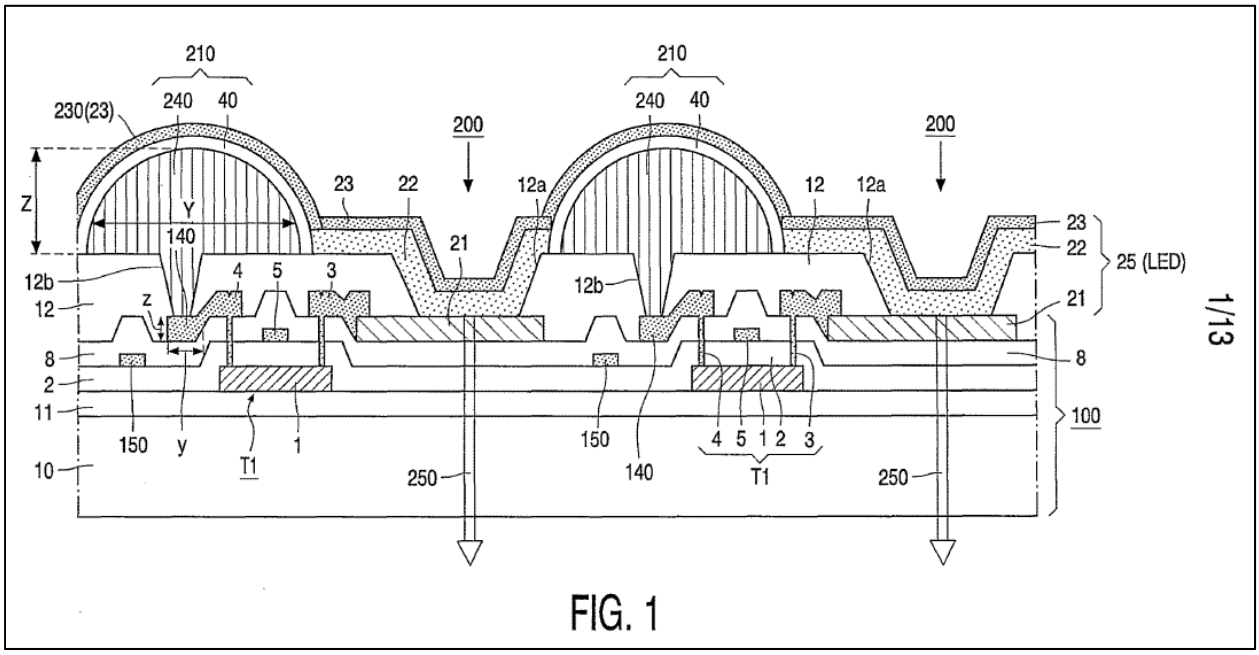


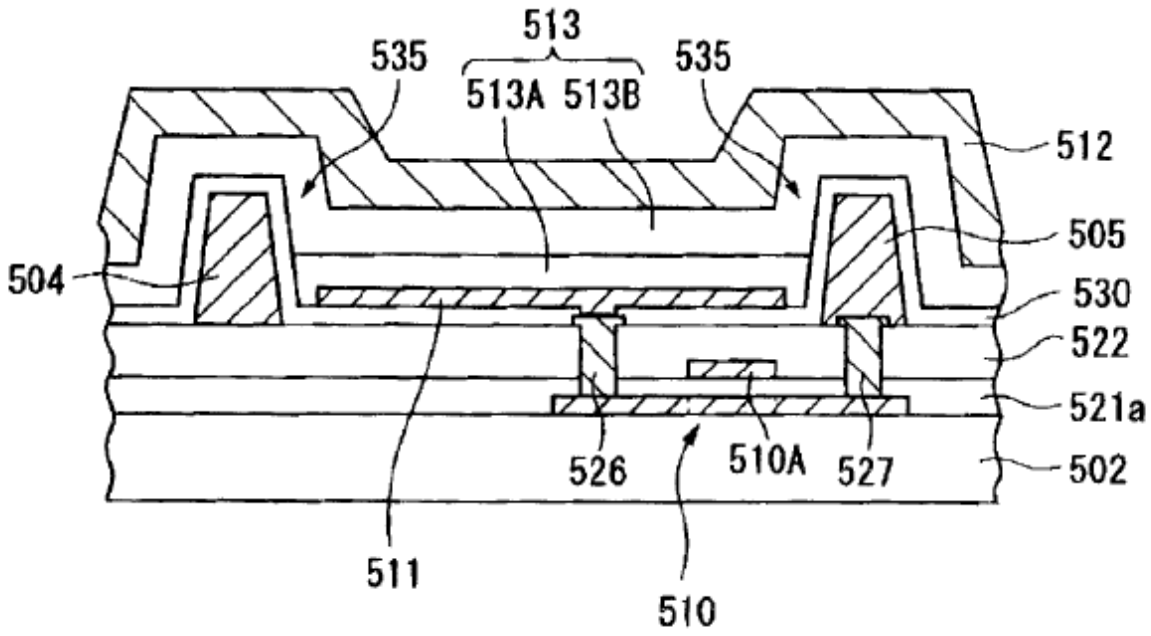
FIG. 1

39. Young similarly discloses such supplemental interconnections to reduce line resistance/voltage drop, explaining that "line resistance can be significantly reduced by using conductive barrier material 240, 240x to replace or to back up a conductor line (for example, 140, 150, or 160) of the circuit substrate 10." Ex. 1011 at 16:5-7.

40. Other prior art references by the September 2004 timeframe of the '338 patent similarly discussed decreasing the resistance of the conductive lines within the OLED structure by increasing their thickness. U.S. Patent Application Pub. No. 2003/0151637 ("Nakamura") (Ex. 1009), for example, disclosed how its "wirings, such as signal line 504, a common electricity supplying line 505, and a scan line

503" were to be "formed in sufficient thickness with regardless of the necessary thickness for wirings," Ex. 1009 at ¶ [0327], as illustrated by Fig. 40 of Nakamura depicting the relatively thick conductive lines 504 and 505:

FIG. 40



c. Pixel Circuit Design in AMOLED Displays

41. As I have noted above, in an active matrix display, each individual pixel contains at least one thin film transistor and a storage capacitor. The TFT substrate, containing the individual TFTs and all the necessary connections and bussing lines, can also be referred to as an "active matrix backplane" or a "transistor array substrate."

42. The backplane is fabricated prior to deposition of the electroluminescent material on the backplane. Due to the high temperatures and etchants involved in fabricating the TFT structures, the active matrix components must be fabricated using semiconductor fabrication technology on a substrate, conventionally made of glass. By using a substrate to build up the TFT and circuit components, the active EL materials can be deposited on the completed substrate using solution or vapor deposition methods.

43. After deposition of the EL material on the backplane, the counter substrate and data driver are attached to complete the module. This process of having the "…OLED device fabricated on the surface of a glass substrate" is illustrated in Fig. 4.1 (b) of Tsujimura (Ex. 1012):

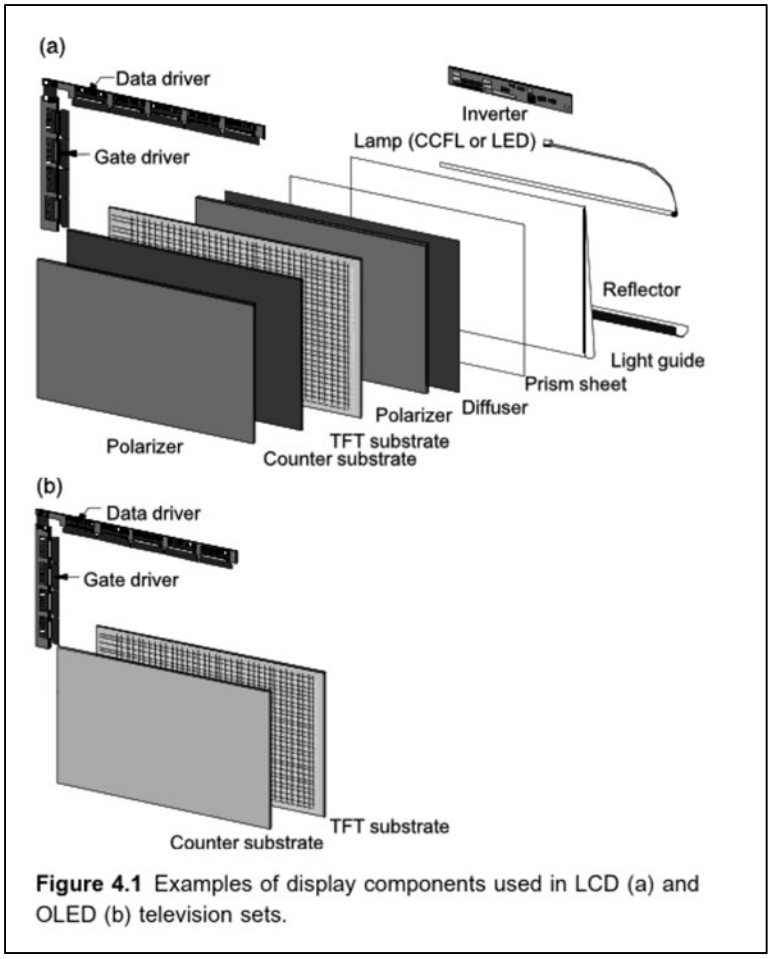


Figure 4.1 Examples of display components used in LCD (a) and OLED (b) television sets.

44. A typical example of the specific steps of fabrication for an OLED are discussed in Crawford (Ex. 1013), which provides the general process steps for a passive matrix PMOLED assembly where the active EL materials are denoted as HITL (Hole Injection and Transport Layer) and LEP (Light Emitting Polymer):

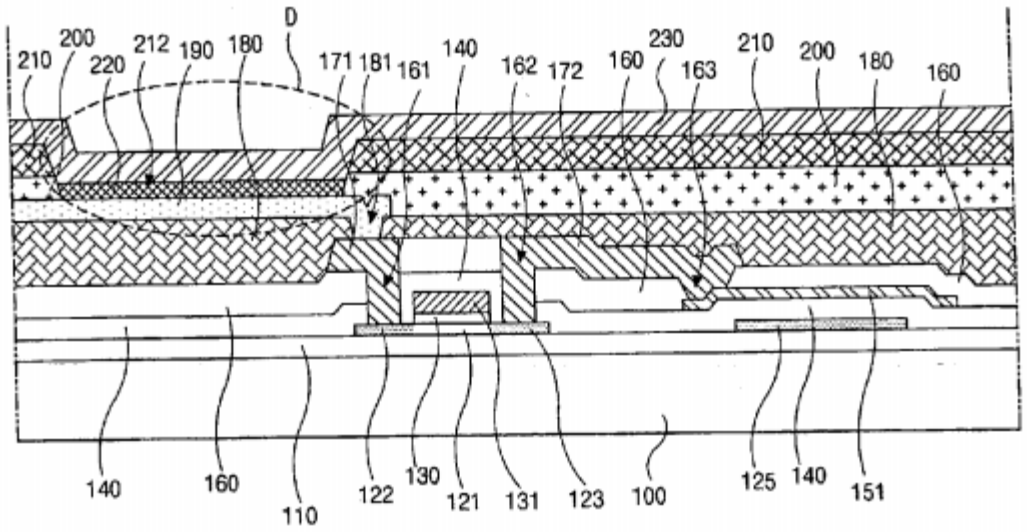
> The fabrication of an OLED onto a composite plastic barrier substrate can be subdivided into three parts. Substrate patterning is the first part and it consists of the following steps:
>
> • deposit and pattern the transparent anode;
> • deposit and pattern the metal bus lines;
> • deposit and pattern any color confinement and/or cathode separating structures that may be used.

> The polymer or active materials are then deposited as follows:
>
> • apply HITL material;
> • apply LEP material.
>
> The device is then completed with these steps:
>
> • deposit and, if needed, pattern the cathode;
> • encapsulate the device.
>
> Ex. 1013 at p. 299.

45. Crawford goes on to observe that "[i]n a plastic AMOLED, an AM array is fabricated on the transparent plastic substrate. The AM array consists of patterned ITO and the TFT circuitry. The active materials can then be applied in the same manner as in a PMOLED." Ex. 1013 at p. 304. The process is very similar in that the circuitry is incorporated into an underlying substrate, and then the active EL material is applied.

46. One example of a AMOLED display structure was disclosed by U.S. Patent Application Publication No. 2003/0127657 to Park (Ex. 1014). Figure 4 of Park illustrates "a cross sectional view of an exemplary active matrix organic electroluminescent display device," Ex. 1014 at ¶ [0034]:

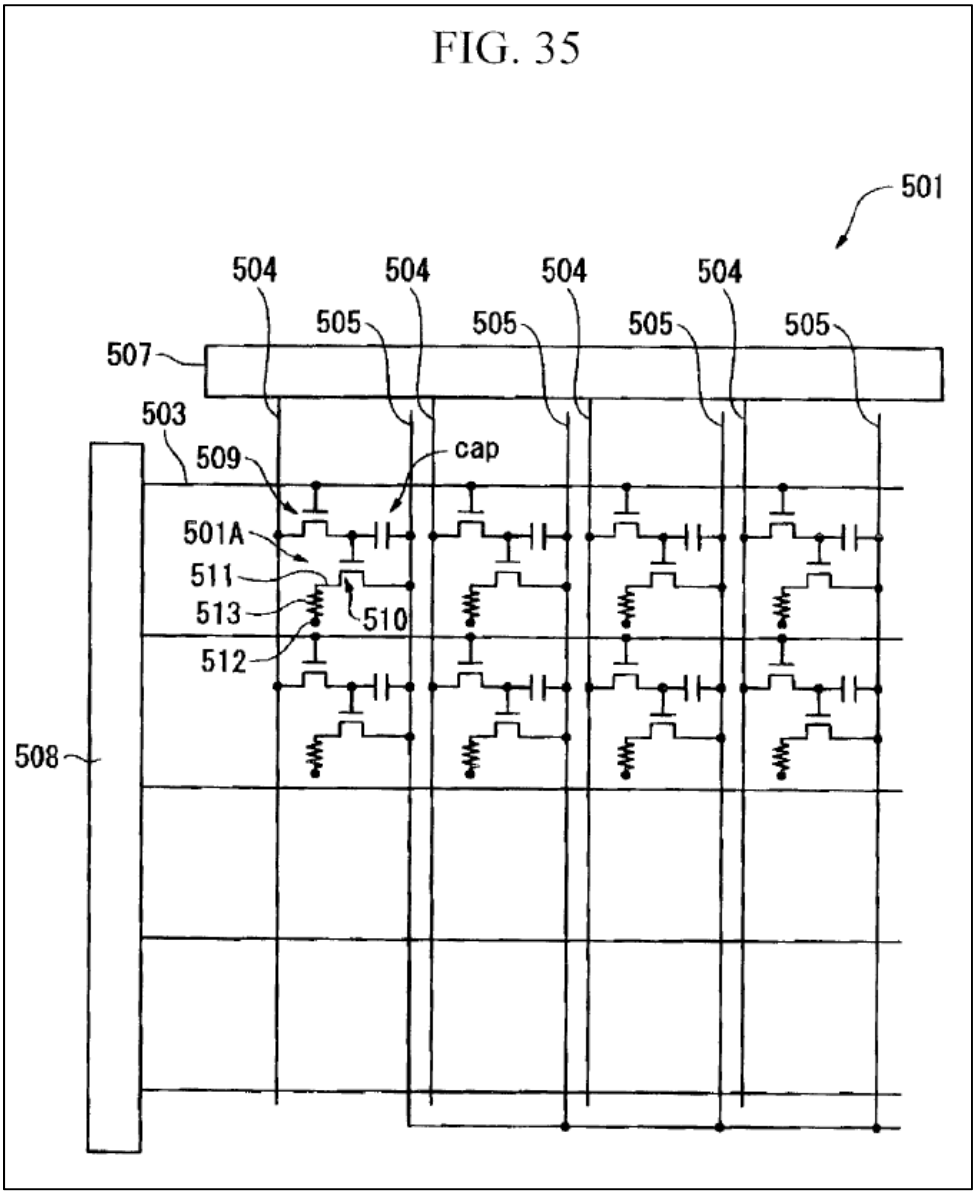
FIG. 4



47. In Park, a thin-film transistor ("drain and source regions 122 and 123" and "gate electrode 131") is formed "on a substrate 100," Ex. 1014 at ¶¶ [0034]-[0035], and the "drain electrode 171 and source electrode 172" connecting to that transistor are covered by insulating "passivation layer 180," Ex. 1014 at ¶ [0036], where that "passivation layer 180" has "a planar upper surface," Ex. 1014 at ¶ [0036]. "A first electrode 190 made of a transparent conductive material may be disposed on the planar upper surface of the passivation layer 180," Ex. 1014 at ¶ [0036], an "organic electroluminescent layer 220," Ex. 1014 at ¶ [0037], with an opaque "second electrode 230" formed on the surface of that organic electroluminescent layer 220," Ex. 1014 at ¶ [0037].

48. By the September 2004 timeframe of the ’338 patent, a number of AMOLED designs had been disclosed in which each individual pixel contained at least two transistors and a storage capacitor. Fig. 35 of Nakamura, for example, illustrated a design in which each “pixel area 501” contained a “switching thin film transistor 509” and a “current thin film transistor 510” connected to “pixel electrode 511,” Ex. 1009 at ¶ [0317]:

FIG. 35



49. Yamazaki described a similar circuit structure for each pixel, in which each pixel contained a "TFT switching element" as well as a "driver element" TFT. Ex. 1006 at ¶ [0005].

50. Hector and Young, too, each disclosed two-transistor circuits for each pixel of their AMOLED displays, with "driving TFT T1" and "addressing TFT T2," as illustrated by Fig. 3 of Hector and Fig. 1 of Young, below, Ex. 1011 at 7:20-32:

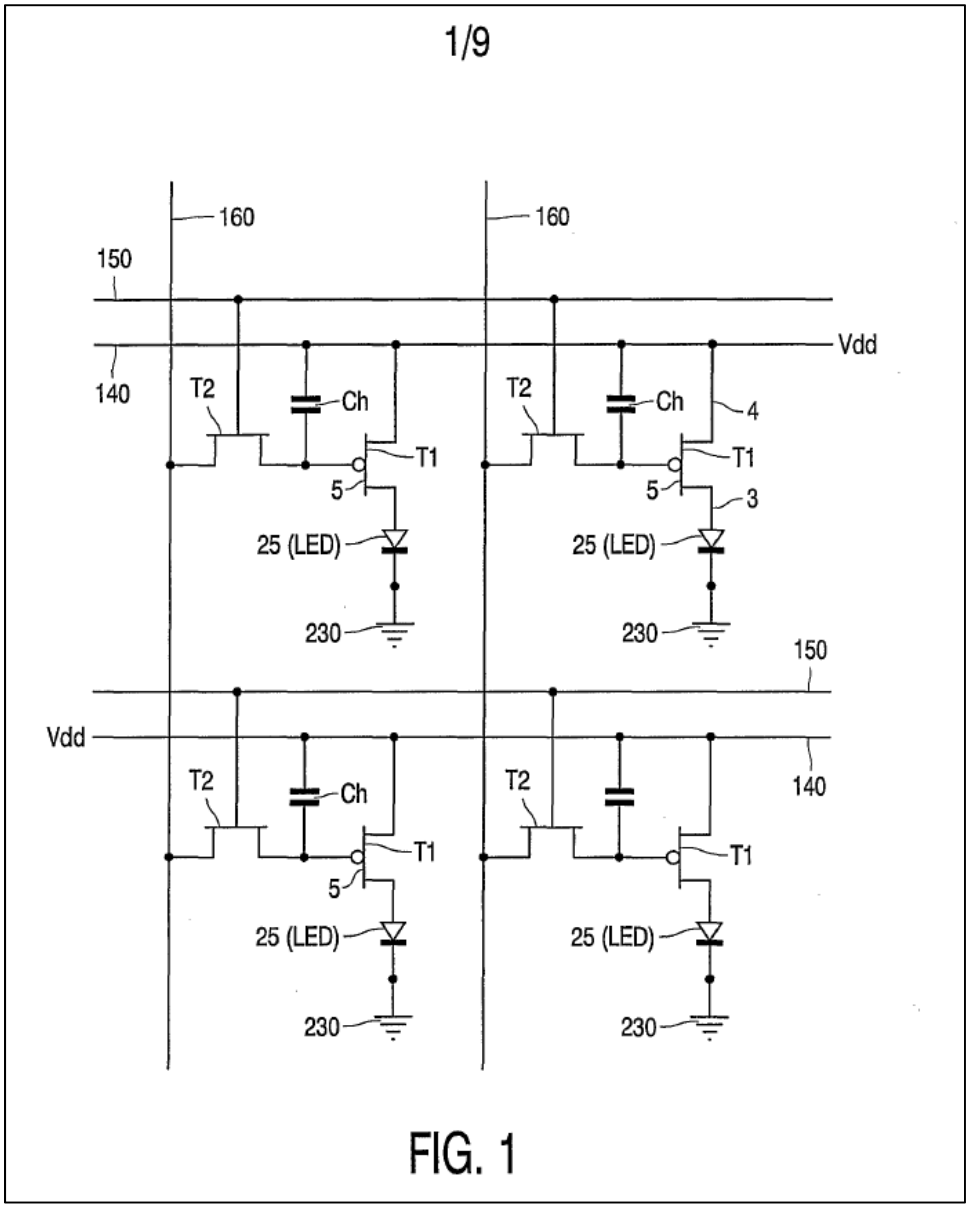


FIG. 1

51. However, by the September 2004 timeframe of the ’338 patent, other pixel circuit designs for AMOLED elements had been developed that featured more than two transistors per pixel. Young, for example, specifically noted that “[o]ther pixel circuit configurations are known for active matrix electroluminescent display devices,” and that “[i]t should be readily be understood that the present invention may be applied . . . regardless of the specific pixel configuration of the device.” Ex. 1011 at 6:3-11.

52. In particular, by September 2004, Casio Computer Co. had repeatedly disclosed a three-transistor pixel circuit configuration for use in AMOLED devices. In U.S. Patent Application Publ. No. 2004/165003 (“Shirasaki II”) (Ex. 1007), published in August 2004, Casio presented a three-transistor circuit structure for each pixel $P_{i,j}$, as depicted in Figures 1 and 3, Ex. 1007 at ¶¶ [0046]-[0047]:

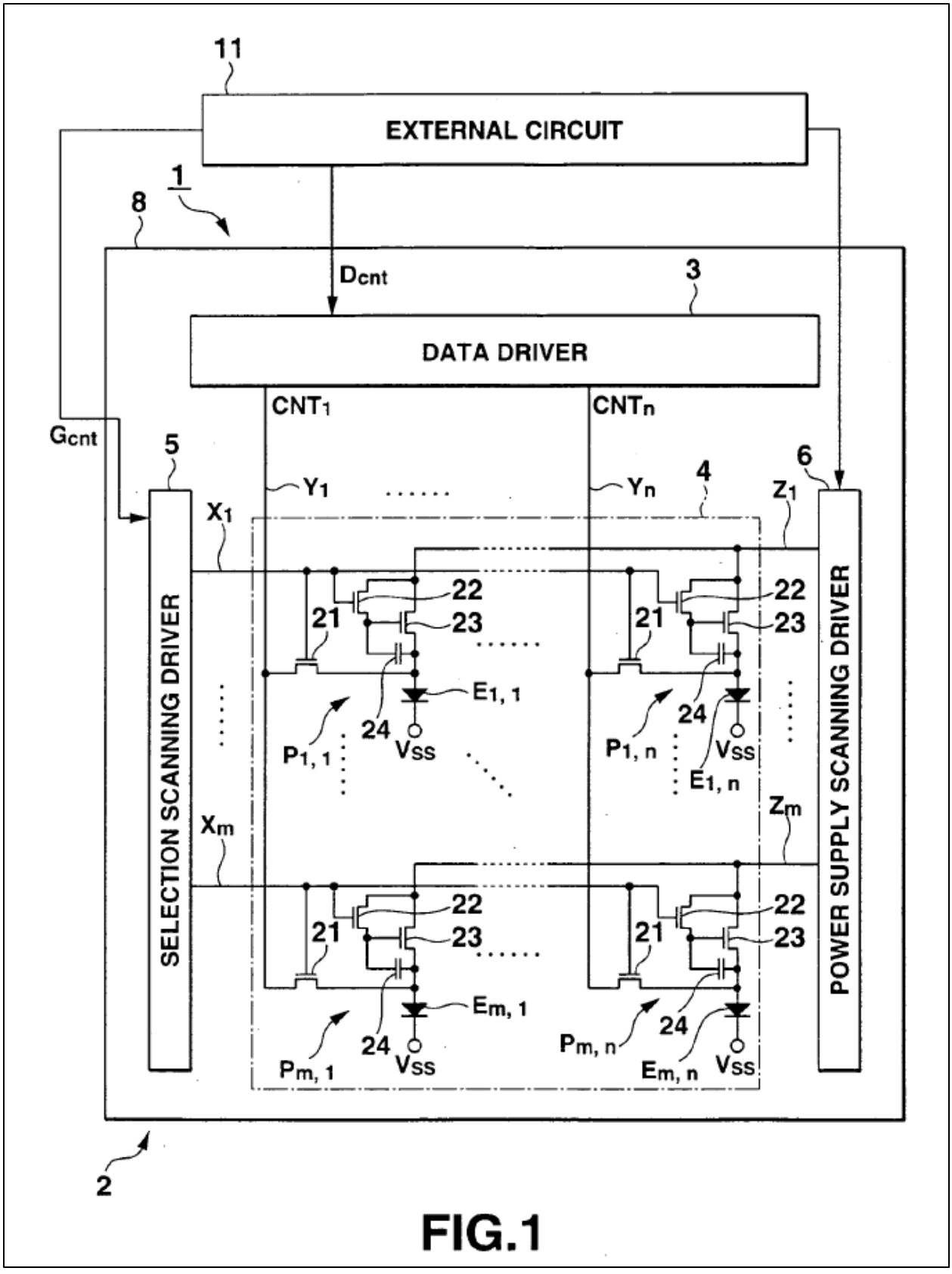


FIG.1

53. Shirasaki II explains that its "pixel circuit . . . drives the organic EL element" in each pixel, and that each "pixel circuit [] comprises the transistors 21, 22, and 23 and a capacitor 24." Ex. 1007 at ¶ [0060]. I note that Shirasaki II's pixel circuit is the same three-transistor pixel circuit that was later used in the figures of the '338 patent, as I discuss further below.

V. OVERVIEW OF U.S. PATENT 7,446,338

a. Summary

54. According to its cover, the '338 patent is entitled "Display Panel," and was filed on September 26, 2005. Ex. 1001 at cover. The '338 patent states, in its "Field of the Invention" section, that "[t]he present invention relates to a display panel using a light-emitting element." Ex. 1001 at 1:14-15. More specifically, the '338 patent goes on to repeatedly note that it is concerned with "organic electroluminescent display panel[s] of [an] active matrix driving type"—in other words, what I have referred to above as an AMOLED. Ex. 1001 at 1:51-65, 3:53-65, 5:51-53.

55. As explained at length above, such AMOLED display panels were well known by the September 2004 timeframe of the '338 patent. Accordingly, the '338 patent does not to purport to be the first to invent the concept of an AMOLED display. On the contrary, in a section entitled "Description of the Related Art," the '338 patent acknowledges that "conventional" AMOLED display panels already

existed. Ex. 1001 at 1:21-26, 1:51-52. The '338 patent further goes on to note that these types of conventional AMOLED display panels each included a number of common, known, elements, including:

- A "transistor array substrate" containing the thin-film transistors (TFTs) that make up the circuit in each pixel of the AMOLED display, Ex. 1001 at 2:17-21;
- An "organic electroluminescent element" (or "organic EL element") "for each pixel" that emits light when a current is supplied to that organic EL element, Ex. 1001 at 1:24-31;
- Electrical "interconnections," for example "a power supply line to supply a current to an organic EL element," Ex. 1001 at 1:51-56; and
- A pixel circuit for each pixel, each circuit containing "driving" and "switching" transistors for each pixel, Ex. 1001 at 1:21-31.

56. The '338 patent notes, however, that because "the thin-film transistor is thin literally," when "a current is supplied from the interconnection to a plurality of light-emitting elements, a voltage drop occurs, or the current flow through the interconnection delays due to the electrical resistance of the interconnection," Ex. 1001 at 1:66-2:30, due to its thin structure as I have discussed above. Accordingly, the '338 patent explains, its goal is to "satisfactorily drive a light-emitting element while suppressing any voltage drop and signal delay." Ex. 1001 at 2:34-36.

57. In addition to noting the resistance/voltage drop issues caused by the thin conductive lines of an OLED structure, the ’338 patent describes how the cathode electrodes of the “organic EL element” also have “a high resistance value” because they are “[c]onventionally . . . formed as a transparent electrode of, e.g., a metal oxide” such as “ITO.” Ex. 1001 at 13:28-14:2. The ’338 patent states that without adding another component, the “only” way to “sufficiently reduce the sheet resistance” of these transparent cathodes is “by increasing the[ir] thickness.” Ex. 1001 at 14:2-3. But, “[w]hen the material [of the transparent pixel electrode] is thick, the transparency of the organic EL element decreases inevitably . . . and the display characteristic becomes poor.” Ex. 1001 at 14:4-7.

58. To solve these issues caused by the relatively high resistance of the thin AMOLED components as described above, the ’338 patent explains that three different types of what the ’338 patent terms “interconnections” can be added to the OLED structure. Ex. 1001 at 21:63-22:61. Each of these three types of “interconnections” has a “low resistance,” and each “interconnection” is designed to be “electrically connected” to components in the OLED structure that have a higher resistance (like the pixel electrodes and conductive lines discussed above) in order to bring down the resistance of those components:

- The “common interconnection” type is electrically connected to the high-resistance cathode electrodes in the OLED element found in each

pixel of the OLED display panel. Ex. 1001 at 22:2-10. The common interconnection lowers the resistance of the cathode electrode, allowing the voltage potential to be "uniform[]" across the cathode electrode and ensuring a uniform appearance across the pixel. Ex. 1001 at 22:2-10.

- The "select" and "feed" interconnection types are each "electrically connected" to the "thin scan lines" and "thin supply lines," respectively, in the OLED structure. Ex. 1001 at 22:20-61. These thicker interconnections reduce the resistance of those thin conductive lines, Ex. 1001 at 22:20-61, and "[w]hen the resistance of these interconnections decreases, the signal delay and voltage drop can be suppressed," Ex. 1001 at 3:63-67.

59. All three types of interconnections described above are depicted in Figure 1 of the '338 patent, which the '338 patent describes as "a schematic plan view . . . of a display panel 1 which is operated by the active matrix driving method." Ex. 1001 at 4:53-56:

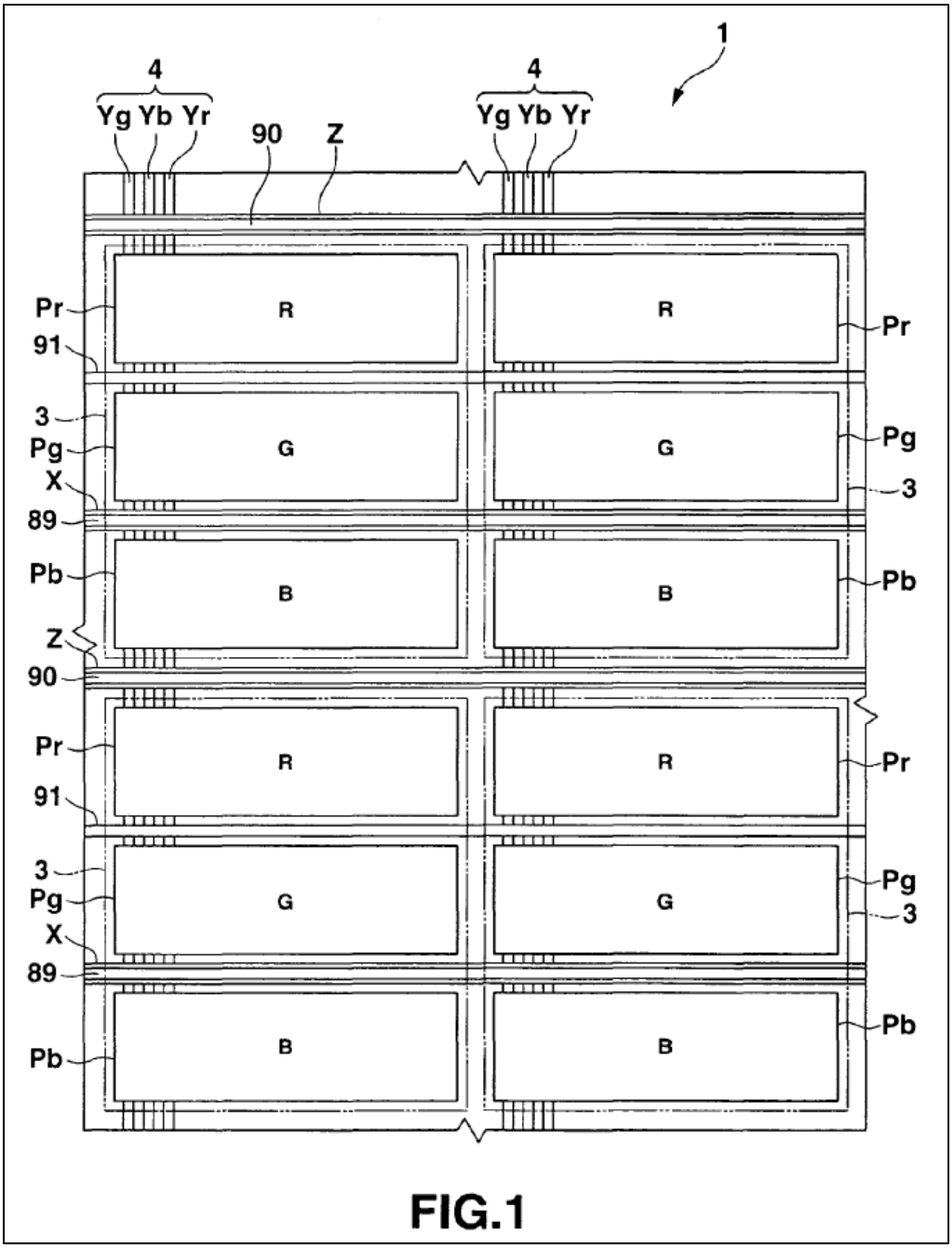


FIG.1

60. Figure 1, above, illustrates "a plurality of select interconnections 89, a plurality of feed interconnections 90, and a plurality of common interconnections 91." Ex. 1001 at 5:23-27. Each of the interconnections is arranged between "sub-pixel[s]" Pr, Pg, and Pb. Ex. 1001 at 5:23-27. The "select interconnection 89

overlaps the scan line X" and is "electrically connected to the scan line." Ex. 1001 at 5:46-50. And the "feed interconnection 90 overlaps the supply line Z" and is "electrically connected to the supply line." Ex. 1001 at 5:46-50.

61. A cross-sectional view of the "layer structure of display panel 1" is depicted by Figure 6 of the '338 patent. Ex. 1001 at 8:18-20. Figure 6 depicts each of these interconnections 89, 90, and 91 being formed on top of what the '338 patent refers to as the "transistor array substrate 50" containing the TFT arrays of the pixel circuit structure. Ex. 1001 at 10:42-47:

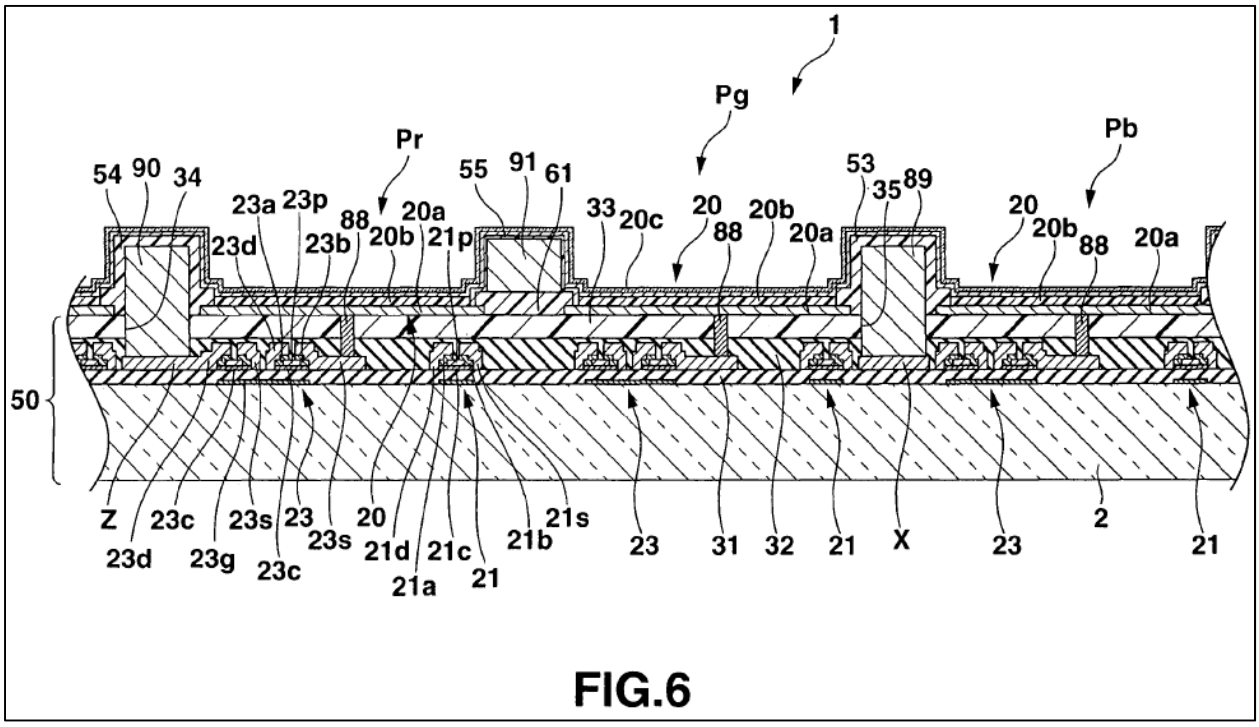


FIG.6

62. The '338 patent states that the "transistor array substrate 50" includes "insulating substrate 2," "gate insulating film 31," "protective insulating film 31,"

and “planarization film 3,” which together form a “layered structure” that contains the “switch transistors 21” and “driving transistors 23.” Ex. 1001 at 10:42-47.

63. The ’338 patent states that “the select interconnections 89 and feed interconnections 90 project upward from the upper surface of the planarization film.” Ex. 1001 at 11:36-41. The “common interconnection 91” is “formed on the insulating line 61.” Ex. 1001 at 10:48-58. The ’338 patent also describes how each one of the “organic EL element[s] 20” is “electrically connected to the . . . source 23s of the driving transistor 23” through “contact hole 88.” Ex. 1001 at 12:6-15. In turn, the “counter electrode 20c functioning as the cathode of the organic EL element 20” is “electrically connected to the common interconnections 91.” Ex. 1001 at 13:28-37.

64. Regarding the pixel circuit structure of the ’338 patent, the patent states that the “transistor array substrate 50” contains three transistors for each red, green, and blue “sub-pixel” of the OLED display panel. Ex. 1001 at 10:25-47. These three transistors are “switch transistor 21,” “holding transistor 22,” and “driving transistor 23.” Ex. 1001 at 10:25-47. Figure 2 of the ’338 patent depicts the “circuit arrangement” of the three transistors that I have cited above, as well as how those three transistors are connected to the “select interconnection 89,” the “feed interconnection 90,” and the “common interconnection 91,” as well as the “organic EL element 20.” Ex. 1001 at 6:45-7:18:

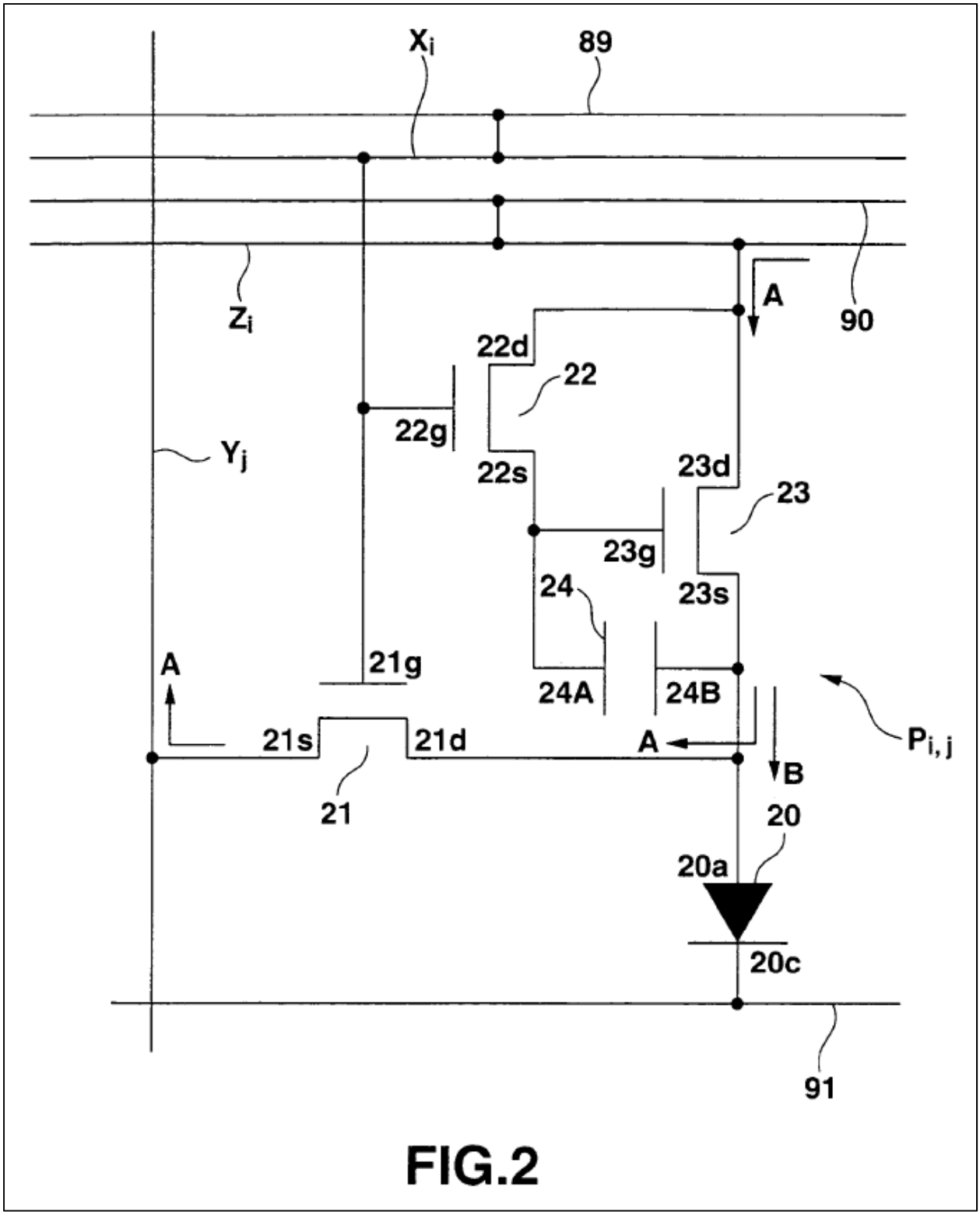


FIG.2

65. The "switching transistor 21 functions to turn on (selection period) and off (light emission period) of the current between the signal line Yj and the source

23s of the driving transistor 23." Ex. 1001 at 17:26-37. That current is illustrated by the arrows "A" in Figure 2 above. Ex. 1001 at 16:30-41. In other words, if the switching transistor is turned on (and current "A" is flowing through it), then "no driving current flows to the organic EL element 20, and no light emission occurs." Ex. 1001 at 17:24-25.

66. The "holding transistor functions to . . . hold the voltage between the gate 23g and the source 23s of the [driving] transistor 23 in the light emission period" (as noted above, the light emission period is when the switching transistor 21 is turned off and current "A" is not flowing, Ex. 1001 at 17:24-37, 16:30-41). Ex. 1001 at 17:29-37. And the "driving transistor 23 functions to drive the organic EL element by supplying a current . . . to the organic EL element 20," causing "the organic EL element [to] emit[] light." Ex. 1001 at 17:29-37, 17:14-15. That "driving current" that is supplied to the organic EL element 20 is illustrated by arrow "B" in Figure 2, above. Ex. 1001 at 17:10-15.

b. File History

67. As part of my preparation of this declaration, I have reviewed the file history for U.S. Application No. 11/235,579, which was the application that led to the '338 patent. Ex. 1001 at cover.

68. When this application was originally filed, claim 1 of the application did not require the three-transistor pixel circuit structure that I discuss above

(requiring the "driving transistor," "holding transistor," and "switch transistor."). Ex. 1002 at 817 (September 26, 2005 originally filed claims). Instead, this claim read as follows:

> 1. A display panel comprising: a transistor array substrate which has a plurality of pixels and is formed by providing a plurality of transistors for each pixel, each of the transistor having a gate, a gate insulating film, a source, and a drain; a plurality of interconnections which are formed to project to a surface of the transistor array substrate and arrayed in parallel to each other; a plurality of pixel electrodes which are provided for each pixel and arrayed between the interconnections on the surface of the transistor array substrate along the interconnections; a plurality of light-emitting layers each of which is formed on each pixel electrode; and a counter electrode which is stacked on the light-emitting layer.

69. Original independent claim 1 was rejected by the Examiner—specifically, over Yamazaki. Ex. 1002 at 446. The Examiner found that this prior art reference disclosed every limitation of independent claim 1, including a "plurality of interconnections which are formed to project to a surface of the transistor array substrate." Ex. 1002 at 446. Specifically, the Examiner wrote that "auxiliary electrode 621" and "auxiliary electrode 721" of this prior art reference disclosed the "plurality of interconnections" of original independent claim 1. Ex. 1002 at 446.

70. Turning to claim 2, however, the Examiner further stated that original dependent claim 2, which recited that the "plurality of transistors includes" "a driving transistor," "a switch transistor," and "a holding transistor," would "be allowable if rewritten in independent form." Ex. 1002 at 448, 817.

71. In response to the Examiner's rejection, the applicants amended independent claim 1 of the application that led to the '338 patent, stating that as amended, independent claim 1 now "incorporate[s] the subject matter of claim 2" (the three-transistor pixel circuit recited by original claim 2). Ex. 1002 at 436 (February 25, 2008 Remarks). After that amendment, the Examiner issued a Notice of Allowance for all of the claims that were still pending in the application. Ex. 1002 at 32-36 (May 30, 2008 Notice of Allowance).

c. The Claims at Issue

72. For the purposes of this declaration, I have been asked to address claims 1-3 and 5-13 of the '338 patent. For reference, I have provided the language of each of those claims below:

> 1. A display panel comprising: a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain; a plurality of interconnections which are formed to project from a surface of the transistor array

substrate, and which are arrayed in parallel to each other; a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate; a plurality of light-emitting layers formed on the pixel electrodes, respectively; and a counter electrode which is stacked on the light-emitting layers, wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

2. A panel according to claim 1, wherein said plurality of interconnections include at least one of a feed interconnection connected to the other of the source and the drain of at least one of the driving transistors, a select interconnection which selects at least one of the switch transistors, and a common interconnection connected to the counter electrode.

3. A panel according to claim 2, wherein each of the light-emitting layers is formed between two of the feed interconnection, the select interconnection, and the common interconnection.

5. A panel according to claim 1, wherein said plurality of pixels include a red pixel, a green pixel, and a blue pixel.

6. A panel according to claim 5, wherein said plurality of pixels comprises a plurality of sets each including the red pixel, the green pixel, and the blue pixel arrayed in an arbitrary order.

7. A panel according to claim 1, wherein at least one of the interconnections has a thickness of 1.31 to 6.00 μm.

8. A panel according to any one of claims 1 or 2 to 7, wherein at least one of the interconnections has a width of 7.45 to 44.00 μm.

9. A panel according to claim 1, wherein at least one of the interconnections has a resistivity of 2.1 to 9.6 μΩcm.

10. A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer that is different from a layer forming the source and the drain of each of the transistors and a layer forming the gate of the transistors.

11. A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer different from a layer forming the pixel electrodes.

12. A panel according to claim 1, wherein said plurality of interconnections are thicker than a layer forming the source and the drain of each of the transistors and a layer forming the gate of each of the transistors.

13. A panel according to claim 1, wherein said plurality of interconnections are thicker than the pixel electrodes.

VI. LEVEL OF ORDINARY SKILL IN THE ART

73. It is my understanding based on my discussion with the attorneys for the Petitioner that factors defining the level of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of technology; and (5) the educational level of active workers in the field.

74. Applying these factors, it is my opinion that a person of ordinary skill in the art at the time of the alleged invention of the ’338 patent (which, as discussed above, is September 29, 2004 (Ex. 1001 at cover)) would have had a relevant technical degree in Electrical Engineering, Computer Engineering, Physics, or the

like, and 2 to 3 years' experience in active matrix display design and electroluminescence.

VII. CLAIM CONSTRUCTION

75. As discussed above, is my understanding that in this proceeding, the claim terms should be given their plain and ordinary meaning as understood by a POSA, consistent with the disclosure and the file history of the '338 patent.

76. After reviewing the '338 patent and the file history, I provide below my understanding of how a POSA would have understood certain claim terms of the '338 patent in light of the '338 patent's disclosure and its file history. I have addressed other claim interpretation issues below when discussing specific claims and the applicability of the prior art to those specific claims.

"transistor array substrate" (claim 1)

77. Regarding the term "transistor array substrate" in claim 1, the '338 patent's specification describes this term as the layered structure upon which the OLED elements (including the pixel electrodes) are formed. The '338 patent states that "the layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50." Ex. 1001 at 10:42-47. The '338 patent also goes on to refer to the surface of "planarization film 33," upon which the pixel electrodes 20a are formed, as "the upper surface of the transistor array substrate 50." Ex. 1001 at 11:50-57.

78. This "transistor array substrate 50" can be seen in Figure 6 of the '338 patent:

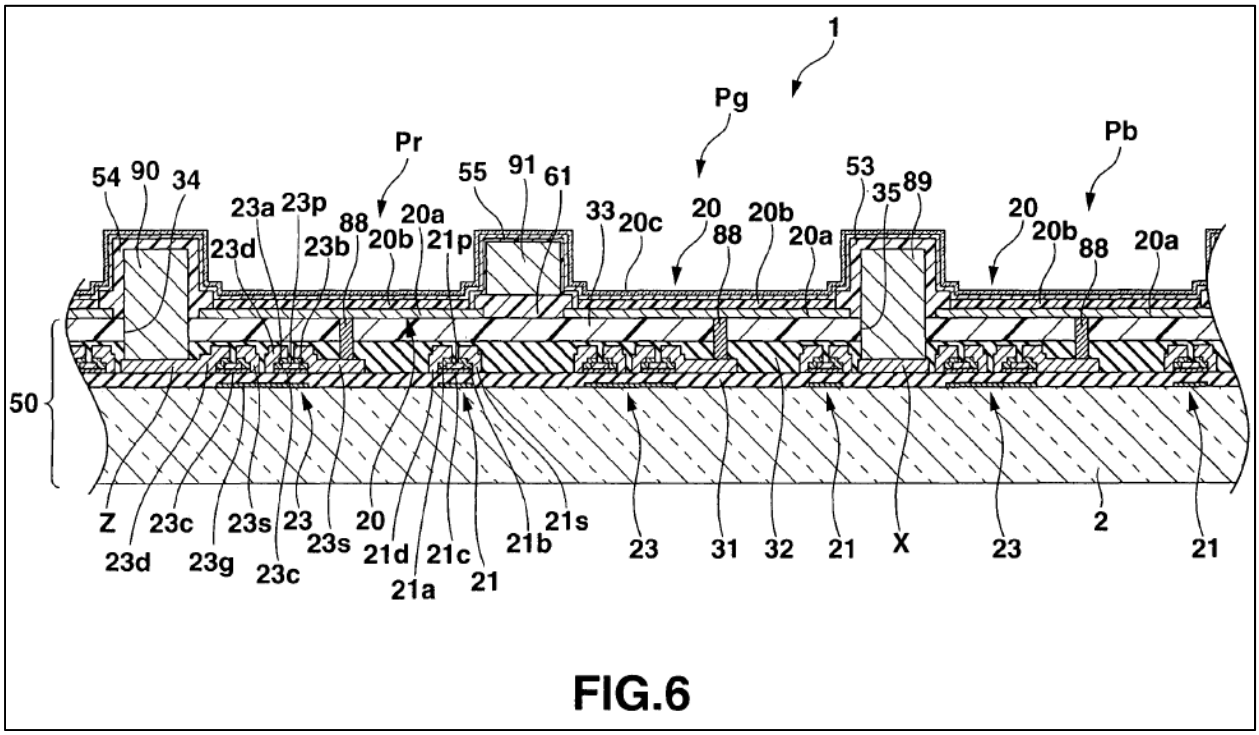


FIG.6

79. As shown by Figure 6, above, the "transistor array substrate 50" includes all of the layers of the OLED structure beneath the pixel electrodes, including any planarization or other insulating layers located above the transistor array and below the pixel electrodes. In Figure 6, for example, the transistor array substrate includes the layers from the insulating substrate 2 through the planarization film 33, including gate insulating film 31 and protective insulating film 32 (as well as transistors 23 and 21 within the transistor array substrate 50).

80. I note that other passages of the '338 patent similarly reinforce that the '338 patent considers the "transistor array substrate" to encompass all of the layers

below the OLED elements 20. For example, the '338 patent repeatedly describes the "upper surface of the planarization film"/"surface of the planarization film" (element 33, above) in the structure depicted in Figure 6 as "the surface of the transistor array substrate." Ex. 1001 at 11:50-55, 10:48-51.

81. To further support my opinion, I note that a separate Casio patent, U.S. Patent No. 7,498,733 ("Shimoda") (Ex. 1015) that shares two of the named inventors as the '338 patent and that was filed on the same day as the '338 patent (September 26, 2005) also refers to a "transistor array substrate 50" and notes (at 8:38-58) that:

> The layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50. In this embodiment, the surface layer of the transistor array substrate 50 is formed from a layered insulating film including the protective insulating film 32 and planarization film 33. The surface layer of the transistor array substrate 50 may include the protective insulating film 32 without forming the planarization film 33. The surface layer of the transistor array substrate 50 may include the planarization film 33 without forming the protective insulating film 32. Another insulating film may be formed on the protective insulating film 32 and planarization film 33.

82. Accordingly, it is my opinion that a POSA at the time of the '338 patent would have understood the claim term "transistor array substrate," consistent with

the disclosure and the file history of the ’338 patent, to encompass a layered structure from an insulating substrate on the bottom through an insulating layer on the top, on whose surface the pixel electrodes of an OLED element are formed.

“a plurality of interconnections which are formed to project from a surface of the transistor array substrate” (claim 1)

83. As I have noted above, the ’338 patent repeatedly describes the claimed “surface of the transistor array substrate” as the upper surface of the uppermost layer of the transistor array substrate, upon which the pixel electrodes of the OLED elements are formed. Ex. 1001 at 11:50-52, 10:48-51. And the ’338 patent provides several examples of what it means for the “plurality of interconnections” to “project from a surface of the transistor array substrate.” Regarding “common interconnection 91,” the ’338 patent explains that this interconnection is formed so that it “project[s] upward from the surface of the planarization film 33.” Ex. 1001 at 10:54-58. And the ’338 patent also states that “the select interconnection 89 and feed interconnection 90 project upward from the upper surface of the planarization film 33.” Ex. 1001 at 11:36-41. Each of these “projecting” interconnection is shown in Figure 6 of the ’338 patent:

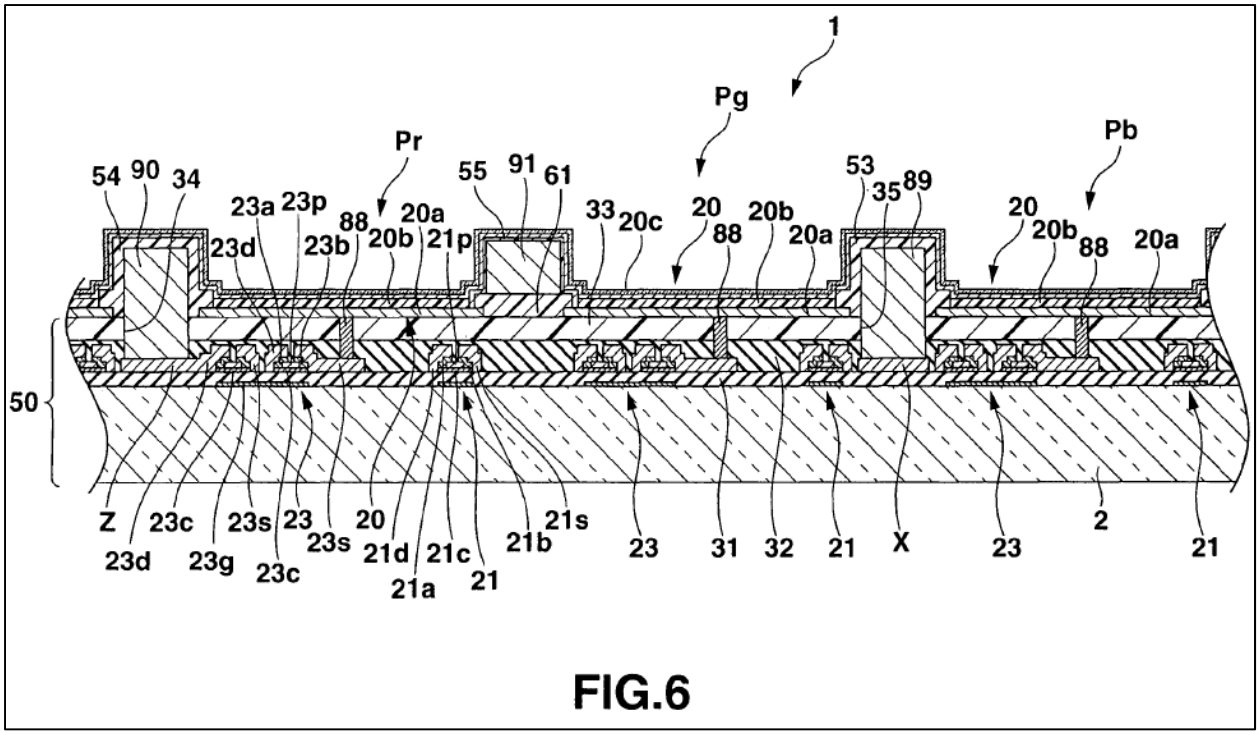


FIG.6

84. Further, the '338 patent also states that all three of "select interconnection 89, feed interconnection 90, and common interconnection 91 . . . are formed . . . to project respect to the surface of the transistor array substrate 50." Ex. 1001 at 12:62-67. Accordingly, it is my opinion that a POSA would have understood this term in claim 1 to encompass any plurality of interconnections which are formed to extend above the upper surface of the topmost layer of the transistor array substrate (for example, layer 33 in Figure 6, above).

"the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate" (claim 1)

85. As I have discussed in the previous two sections, the '338 patent repeatedly describes how the "surface of the transistor array substrate" refers to the

upper surface of the uppermost insulating layer upon which the pixel electrodes of the OLED elements are formed. Ex. 1001 at 11:50-52, 10:48-51. Given these descriptions from the '338 patent, it is my opinion that a POSA would have understood the limitation "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate" to require both that: a) the pixel electrodes be arrayed along the interconnections between the interconnections; and b) the pixel electrodes be arrayed on the surface of the transistor array substrate (in other words, on the surface of the topmost insulating layer of the transistor array substrate).

86. My interpretation of this claim term is supported by the disclosure and the claims of the '338 patent. I note that the '338 patent specifically recites, in the specification, that "[t]he plurality of sub-pixel electrodes 20*a* are arrayed in a matrix on the upper surface of the planarization film 33, i.e., the upper surface of the transistor array substrate." Ex. 1001 at 11:50-52. I also note that Figure 6 of the '338 patent displays these sub-pixel electrodes 20a being arrayed along and between the interconnections 89, 90, and 91:

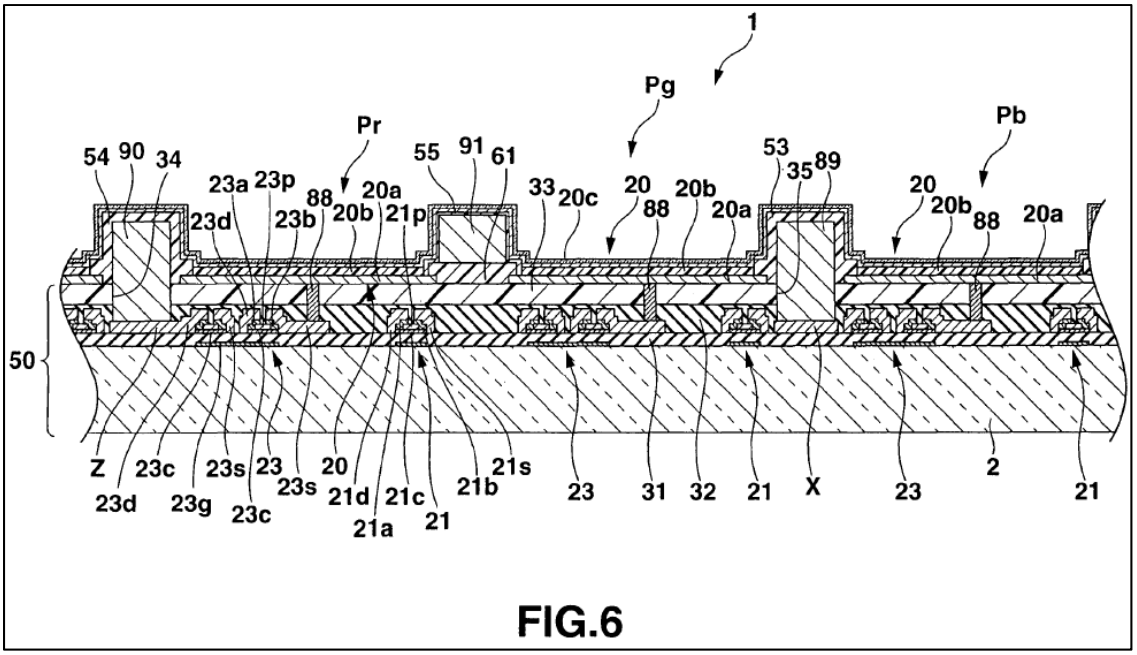


FIG.6

VIII. OVERVIEW OF THE PRIOR ART

a. Kobayashi (US Patent Application Pub. No. 2002/0158835) (Ex. 1003)

87. Kobayashi is a publication of a U.S. patent application. Ex. 1003 at cover. Like the '338 patent, Kobayashi is directed to the field of AMOLED display panels. More specifically, Kobayashi explains that its "invention relates to a planar display device such as an organic electroluminescence (EL) display device," and "[i]n particular . . . to an active matrix type planar display device." Ex. 1003 at ¶ [0002]. Kobayashi is especially focused on using an "auxiliary electrode" which is "electrically connected to" the transparent cathode for each of the organic EL elements in the pixels of the AMOLED display, which allows "the resistance of the entire [transparent cathode] can be lowered, and non-uniformity in display within the display screen can sufficiently be suppressed." Ex. 1003 at ¶¶ [0061]-[0062].

88. In Figure 1, Kobayashi illustrates "the structure of an organic EL display device," Ex. 1003 at ¶ [0040]:

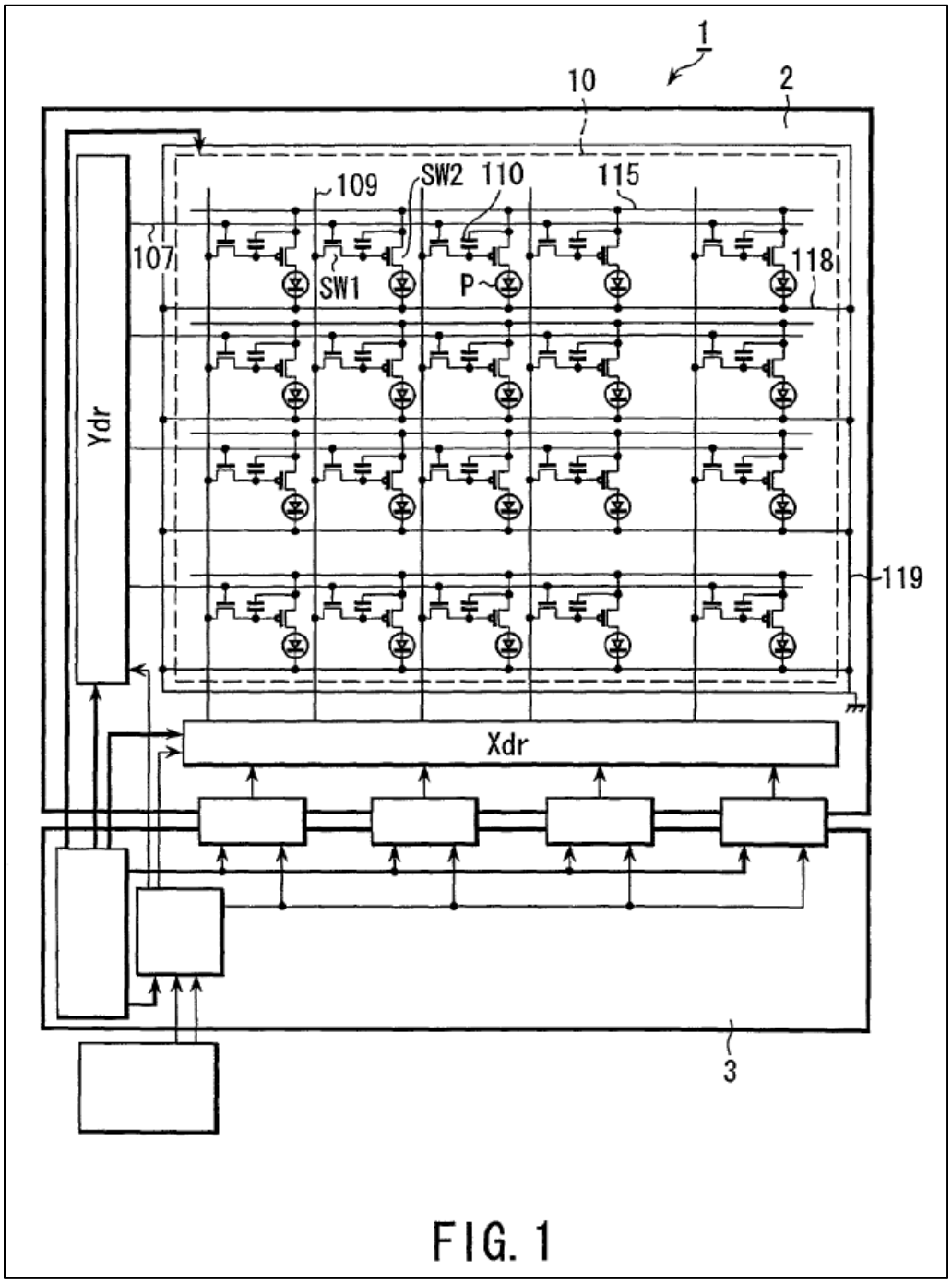


FIG. 1

89. This "[o]rganic EL panel 2 comprises three kinds of display elements P, which respectively emit red, green, and blue light," and which "are arranged in a

matrix." Ex. 1003 at ¶ [0041]. Each "organic EL display element P" in the panel "is connected to two thin-film transistors (TFTs): a first "TFT functioning as a switching element SW1," and a second "TFT functioning as a driving control element SW2." Ex. 1003 at ¶ [0043]. Kobayashi's "organic EL display device" "includes auxiliary wiring elements 118" which are arranged "in a lattice shape so as to surround . . . each display element P." Ex. 1003 at ¶ [0046].

90. Kobayashi explains that Figure 7 depicts an example of the layered "structure of the organic EL display device 1," Ex. 1003 at ¶ [0087]:

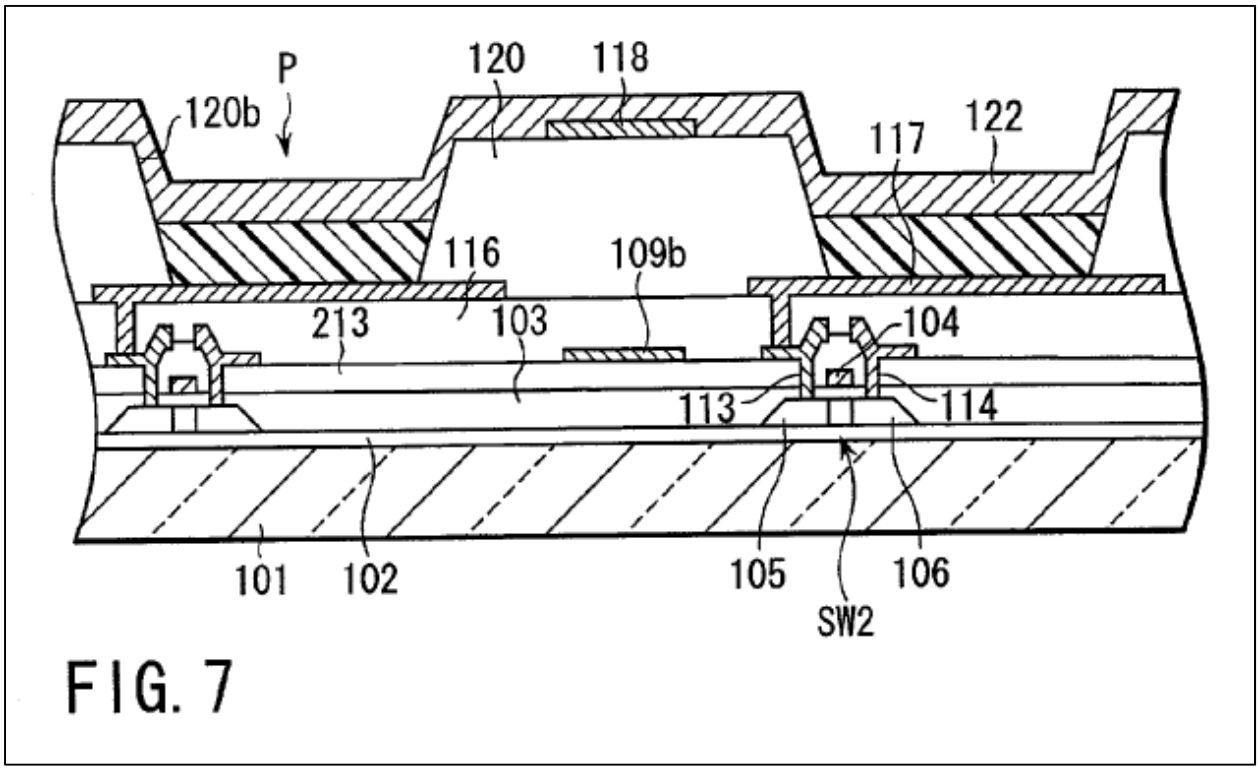


FIG. 7

91. Kobayashi explains that thin-film transistors SW1 and SW2 are used to create "circuit[s] formed on the support substrate 101." Ex. 1003 at ¶ [0084]. The support substrate 101 is itself made out of "glass, etc." Ex. 1003 at ¶ [0064]. On

top of the TFTs SW1 and SW2 is layered an "insulating layer 116," Ex. 1003 at ¶ [0060], which is made out of a silicon nitride "film," Ex. 1003 at ¶ [0073], and that is layered "over the TFTs . . . and [the] wiring under the insulating layer 116," Ex. 1003 at ¶ [0060]. After the insulating layer has been laid down over the TFT circuit, the "first electrode 117 of display element P is [then] disposed on the insulating layer 116." Ex. 1003 at ¶ [0074].

92. Kobayashi further explains that in the layered OLED structure of Figure 7 depicted above, the "auxiliary wiring elements 118" that are the focus of Kobayashi are designed to be "electrically connected to the second electrode 122" and are therefore "disposed in a lattice shape on partition walls 120 that electrically isolate the pixels in the display region" of the AMOLED display panel. Ex. 1003 at ¶ [0088]. Because the material from which auxiliary wiring element 118 is formed has a lower resistance than the material from which transparent cathode electrode 122 is formed, as Kobayashi describes in paragraph [0105], Kobayashi explains that "[b]y electrically connecting the arranged auxiliary wiring elements 118 and second electrode 122, non-uniformity in voltage within the screen due to the resistance of the second electrode 122 can be suppressed . . . and the quality in display enhanced," Ex. 1003 at ¶ [0090].

b. Shirasaki (U.S. Patent Application Pub. No. 2004/0113873) (Ex. 1004)

93. Shirasaki is a publication of a U.S. patent application by the same inventor as the lead named inventor of the '338 patent (Tomoyuki Shirasaki), and I note that the "assignee" listed on both the '338 patent and Shirasaki is the same (Casio Computer). Ex. 1004 at cover. Shirasaki, like the '338 patent, is directed to AMOLED type display panels—Shirasaki describes "an active matrix type light emitting panel," Ex. 1004 at ¶ [0041], which contains "a plurality of organic EL elements [that] are arrayed in a matrix manner on [a] transparent substrate," Ex. 1004 at ¶ [0043].

94. Shirasaki's disclosure is particularly focused on the same three-transistor pixel circuit structure that was added to and resulted in allowance of independent claim 1 of the '338 patent. Shirasaki discloses that same three-transistor pixel circuit structure in Figure 5B (for example), which includes what the '338 patent refers to as a "driving transistor" (transistor 12 in Shirasaki), "switch transistor" (transistor 11 in Shirasaki), and "holding transistor" (transistor 10 in Shirasaki):

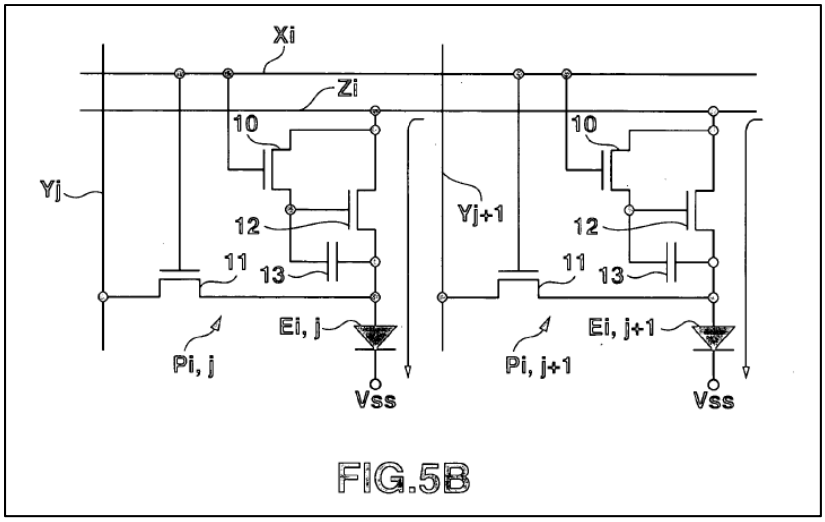


FIG.5B

95. Shirasaki explains that this three-transistor pixel circuit structure, which was later re-used in the '338 patent, was an improvement over "conventional light emitting element displays," in which commonly only "two transistors are formed in each pixel" (such as Kobayashi and the other conventional two-transistor pixel circuit structures that I have described above). Ex. 1004 at ¶¶ [0003]-[0004], Figure 11. Shirasaki explains that its three-transistor pixel circuit ensures that the pixels of its AMOLED display "stably display images with desired luminance in a display panel." Ex. 1004 at ¶¶ [0011]-[0012], [0094].

c. Childs (International Publication No. WO 03/079441)

96. Childs is a publication of an international PCT application. Like the '338 patent (and Kobayashi and Shirasaki), Childs' disclosure is focused on AMOLED display panels, or as Childs describes: "active-matrix display devices, particularly but not exclusively electroluminescent displays using light-emitting diodes of semiconducting conjugated polymer or other organic semiconductor

materials." Ex. 1005 at 1:5-7. Childs' disclosure is particularly focused on a specific feature in its AMOLED structure: "conductive barrier material 240 that is used as an interconnection" in its AMOLED display. Ex. 1005 at 6:25-29, 4:19-21. These conductive barrier materials 240 are each "connected with a circuit element" and are designed to lower/reduce the resistance of that connected circuit element in order to "reduce voltage drops" along those circuit elements. Ex. 1005 at 3:17-25.

97. Figure 1 of Childs illustrates the "pixel circuit configuration" of the pixel circuits in Childs' OLED, with each pixel circuit containing a "drive" thin-film transistor T1 and an "addressing" (i.e., switching) thin-film transistor T2. Ex. 1005 at 7:1-17:

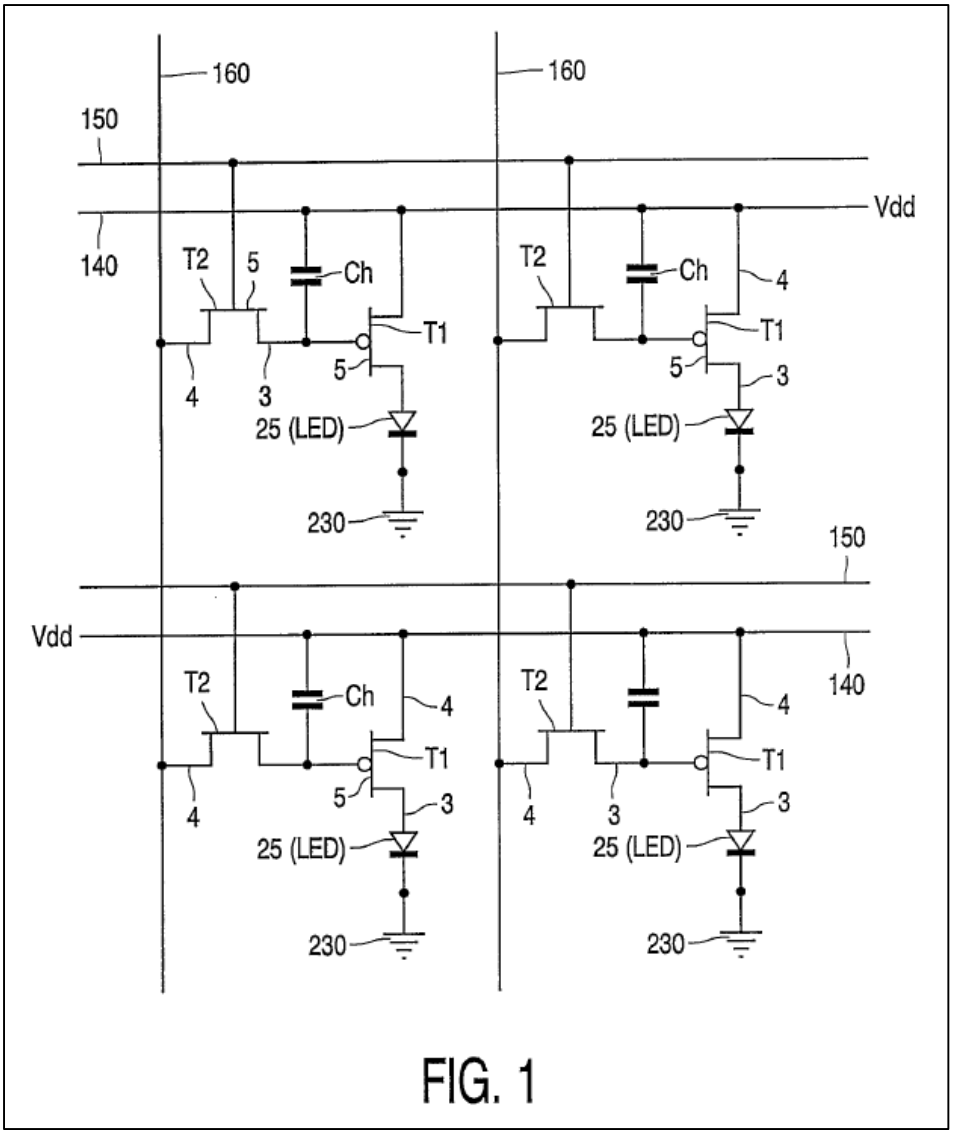


FIG. 1

98. In Figure 2, Childs provides a "cross-sectional view of part of the pixel array and circuit substrate" (the layers of its AMOLED display panel), Ex. 1005 at 5:6-9:

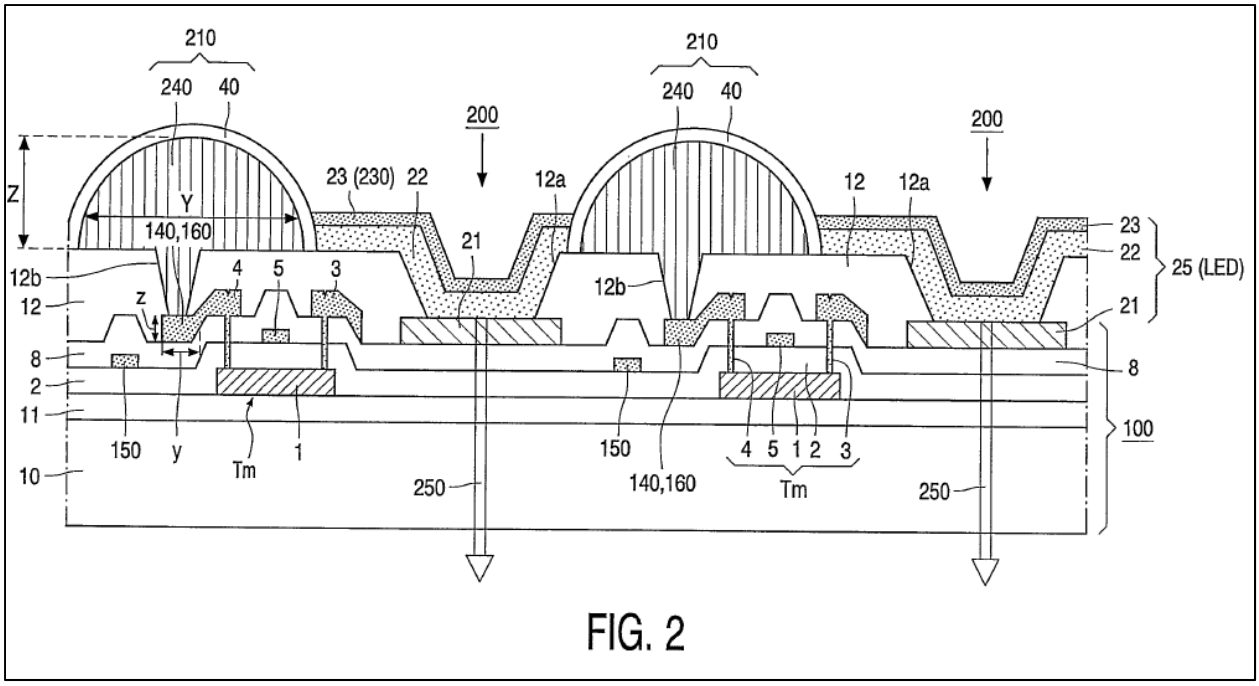


FIG. 2

99. Childs provides a further description of this layered structure, explaining that the TFT circuits are contained within "circuit substrate 100," which begins with "insulating glass base 10" and extends through the "planar insulating layer 12." Ex. 1005 at 7:31-8:27. On top of the surface of planar insulating layer 12, Childs forms "pixel barriers 210," which act as "dams" that separate and prevent overflow of a polymer solution between the respective areas of the individual pixels 200" (the polymer solution being the OLED material 22) while those "polymer layers 22" (the OLED elements) are being deposited ("ink-jet printed or spin-coated for the pixels 200," Ex. 1005 at 15:29-31), Ex. 1005 at 8:28-9:17.

100. These "pixel barriers 210" incorporate "conductive barrier material 240 that is used as an interconnection." Ex. 1005 at 6:25-29. These conductive "interconnections" 240 are "preferably" formed from metal, Ex. 1005 at 10:6-8, and

the interconnections "are connected to and/or from one or more circuit elements of the circuit substrate 100," such as "supply line 140" and/or "signal line 160," Ex. 1005 at 9:18-29. Childs further discloses that because the conductive metal of the interconnections 240 has a "very low resistivity," Ex. 1005 at 10:6-10, the conductive lines to which the conductive interconnections are electrically connected (such as the supply lines and/or signal lines) will have their resistance "significantly reduced," Ex. 1005 at 10:25-27, 13:3-6. Childs notes that the design of these conductive interconnections will accordingly result in "reduc[ing] voltage drops along" those supply lines or signal lines (or any other conductive elements to which the interconnections are electrically coupled). Ex. 1005 at 3:17-25.

IX. THE COMBINATION OF KOBAYASHI AND SHIRASAKI (CLAIMS 1-2, 5-6, 9-11)

101. Kobayashi and Shirasaki each come from the same technological field: the structure of an AMOLED display panel. Accordingly, in this particular case, a POSA would have looked to the disclosures of these references together when designing an AMOLED display panel.

102. The particular combinations of Kobayashi and Shirasaki's features that a POSA would have had reason to make, and his or her reasons for making these combinations, are discussed in further detail below. However, in summary, my analysis below concludes that a POSA would have been motivated to and readily capable of combining the features in Kobayashi and Shirasaki to arrive at what is

claimed in the ’338 patent based on the disclosures in the prior art and a POSA’s knowledge of the art in the September 2004 timeframe of the ’338 patent.

a. Independent Claim 1

1[preamble]: A display panel comprising:

103. Kobayashi discloses a display panel. Specifically, Kobayashi states that its invention is directed to “a planar display device such as an organic electroluminescent (EL) display,” and, “[i]n particular . . . an active matrix type planar display device.” Ex. 1003 at ¶ [0001]. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

1[a]: a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain;

104. A POSA would have recognized that Kobayashi discloses the claimed “transistor array substrate.”

105. As I have explained above in my discussion of the proper claim construction for this claim element, a POSA, in accordance with the disclosure and claims of the ’338 patent, would have understood this claim element to encompass a layered structure from a bottom substrate through a topmost insulating layer, upon whose surface the pixel electrodes are formed. I noted above that the ’338 patent’s specification states that “the layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50,” Ex. 1001 at 10:42-47,

and refers to "the upper surface of the planarization film 33, i.e., the upper surface of the transistor array substrate 50," Ex. 1001 at 11:50-55.

106. A POSA would have recognized that Kobayashi's layered structure that extends from the "insulating support substrate 101 of glass, etc.," Ex. 1003 at ¶ [0064], through the uppermost "insulating layer 116" formed from SiNx film," Ex. 1003 at ¶ [0073], corresponds to the claimed "transistor array substrate," as illustrated by Figure 7 of Kobayashi:

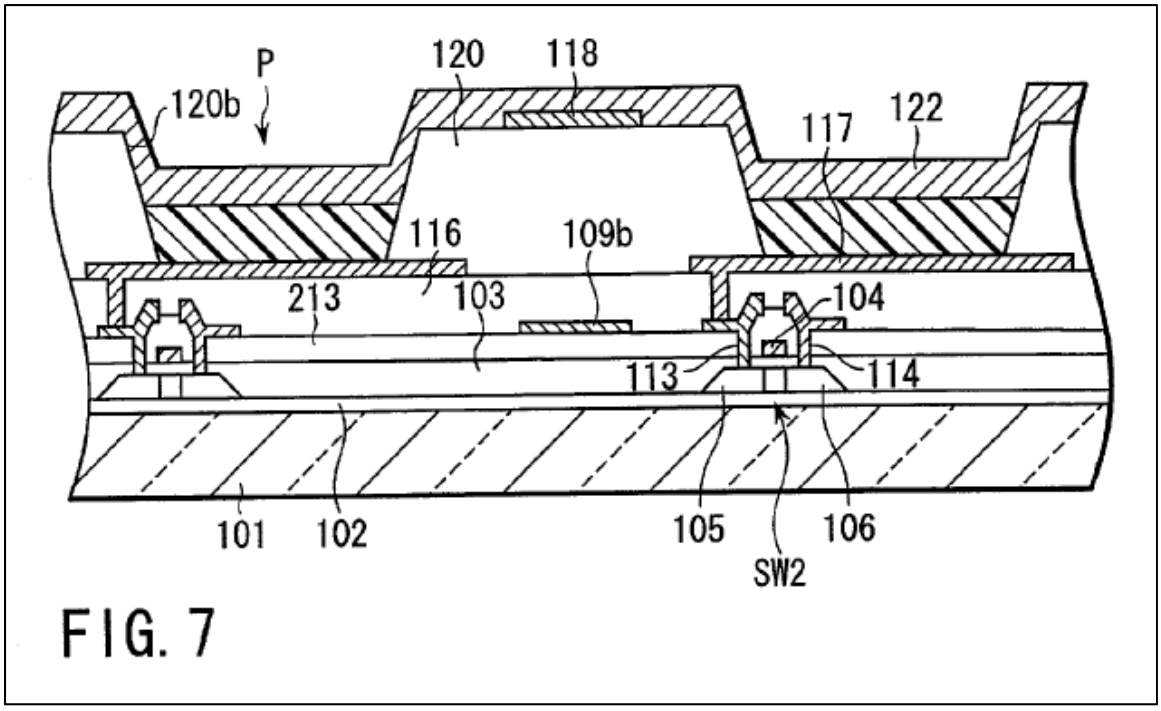


FIG. 7

107. A POSA would have recognized that Kobayashi's "support substrate 101" corresponds to the '338 patent's "insulating substrate" on the bottom of the claimed transistor array substrate, and that "Kobayashi's "insulating layer 116," which Kobayashi describes as a "film" that creates a "plane" upon which the "first

electrodes 117" are formed, Ex. 1003 at ¶ [0080], corresponds to the topmost insulating layer of the claimed "transistor array substrate."

108. Furthermore, a POSA would also have recognized that Kobayashi's layered structure from the bottommost support substrate 101 through the uppermost insulating layer 116 additionally: (a) includes a plurality of pixels; and (b) comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain:

"includes a plurality of pixels"

109. Kobayashi states that its "organic EL panel 2 comprises three kinds of display elements P" (where a POSA would have understood P to represent "pixel," as Kobayashi elaborates in paragraphs [0090]-[0091]), and that each of these pixels respectively emit red, green, and blue light" and "are arranged in a matrix" in "display region 10." Ex. 1003 at ¶ [0041]. This is illustrated by Fig. 1 of Kobayashi:

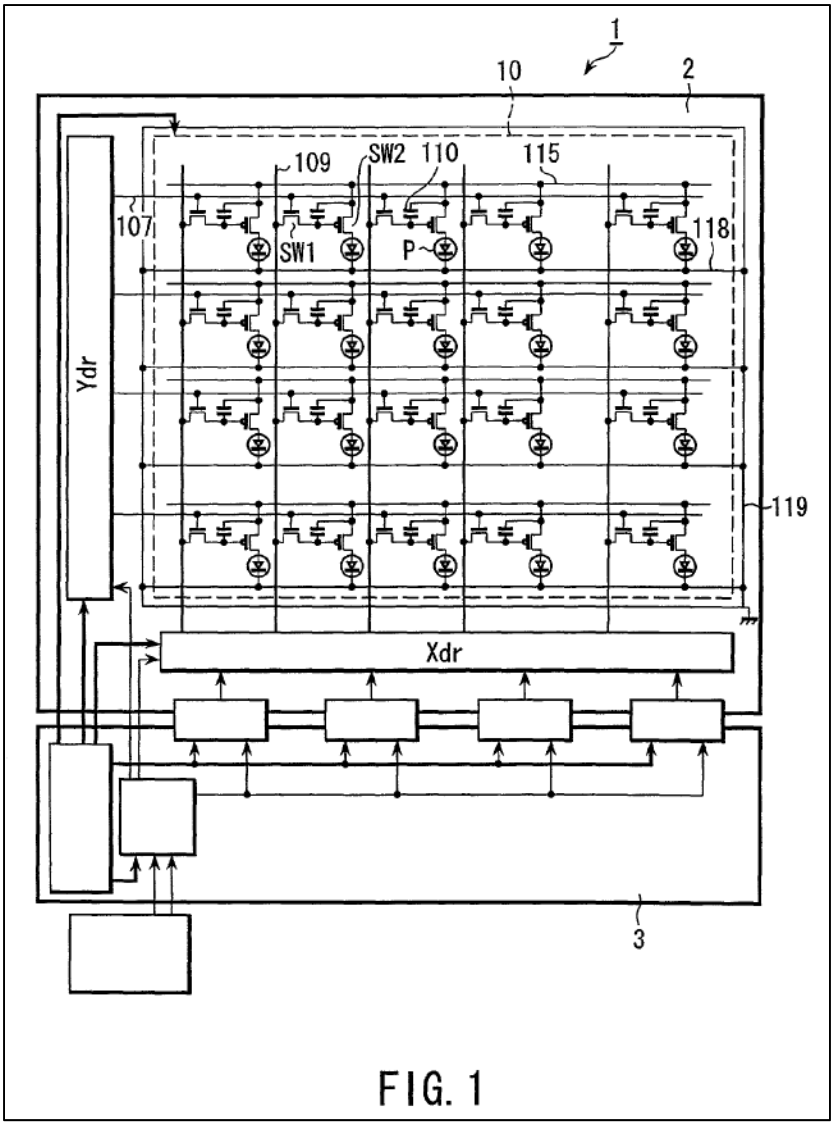


FIG. 1

110. Kobayashi further elaborates that display elements P are each "pixels," describing how "the auxiliary wiring elements 118 [are] arranged in a lattice shape" "to surround the pixels of all display elements P." Ex. 1003 at ¶¶ [0090]-[0091]. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

"comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain"

111. Kobayashi also discloses that its layered structure that corresponds to the claimed transistor array substrate comprises a plurality of transistors for each pixel. As Figure 1 illustrates, in each "organic EL display element P" (in other words, in each pixel), "the organic EL panel 2 includes an n-type TFT functioning as a switching element SW1" and "a p-type TFT functioning as a driving control element SW2," Ex. 1003 at ¶ [0043]:

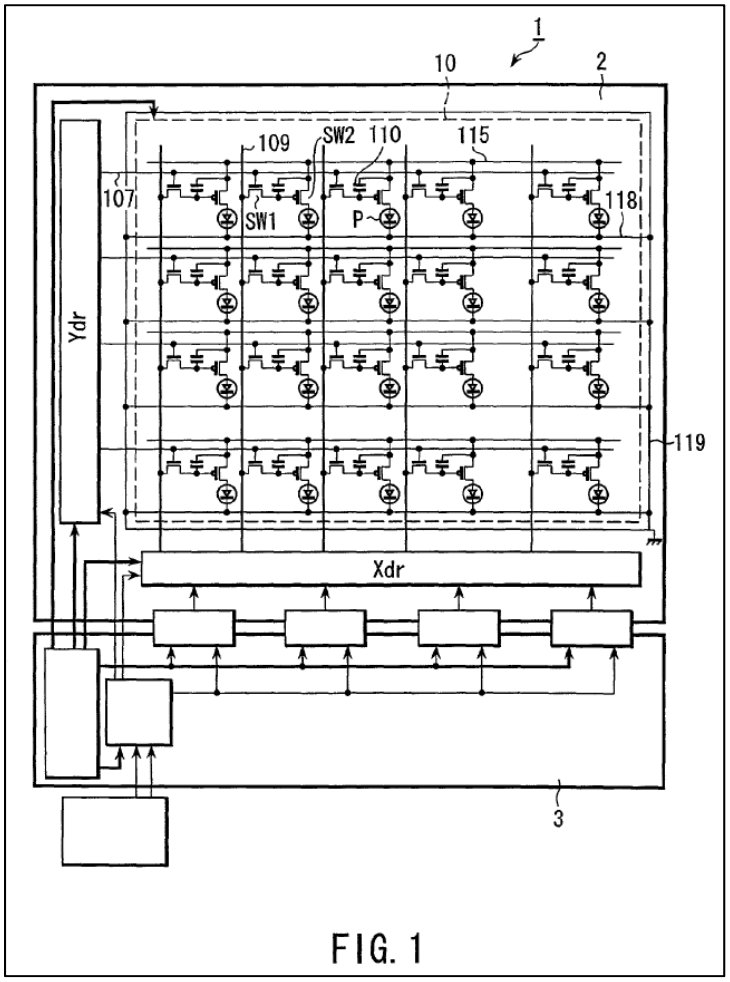


FIG. 1

112. Kobayashi also explains that these thin-film transistors SW1 and SW2 are found within its transistor array substrate, stating that the pixel "circuit [is]

formed on the support substrate 101," Ex. 1003 at ¶ [0084], and "under the insulating layer 116," Ex. 1003 at ¶ [0060].

113. Kobayashi's Figure 7 depicts how TFT SW2 is located within the transistor array substrate (I note that the other transistor in the pixel circuit, SW1, would also be located in this same plane in the transistor array substrate, but is not shown in this particular cross-sectional view):

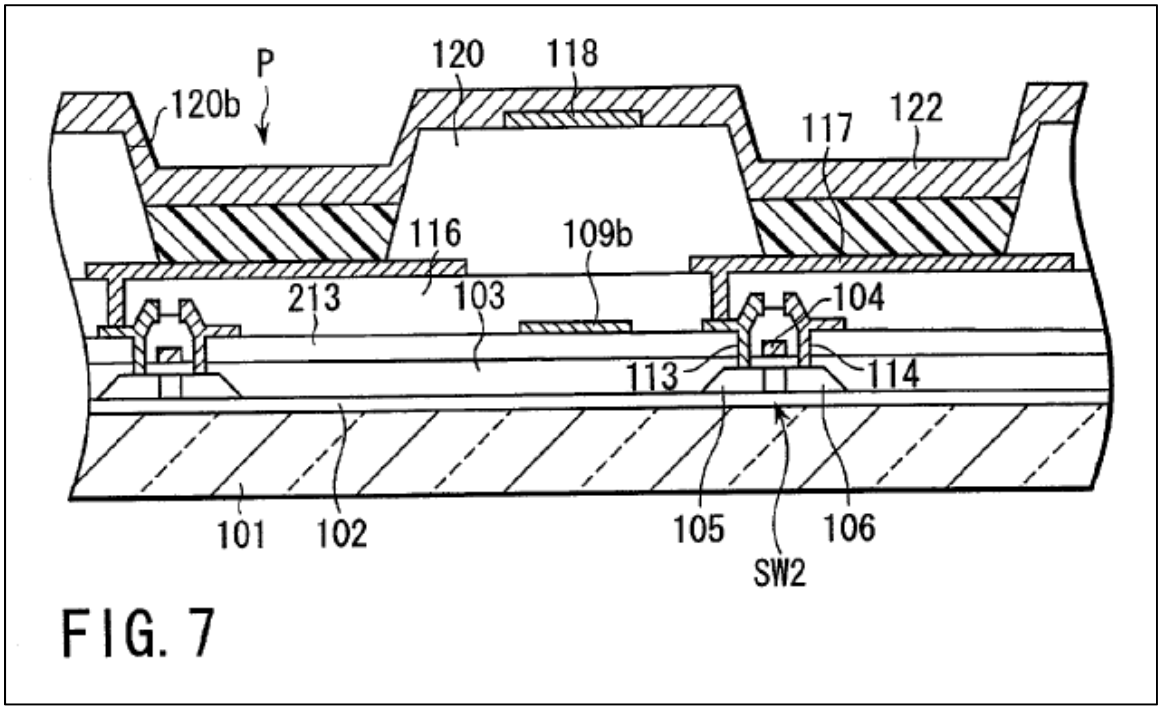


FIG. 7

114. Kobayashi discloses (and Figure 7 illustrates) that each transistor SW2 is made up of "a source region 105" (and connected "source electrode 113"), "[a] drain region 106" (and connected "drain electrode 114"), "a gate insulating film 103," and "a gate electrode 104," as illustrated above. Ex. 1003 at ¶¶ [0066], [0070]. Kobayashi similarly discloses that each transistor SW1 is made up of "a source

region 111" (and connected "source electrode 132"), "a drain region 112" (and connected "drain electrode 131"), "a gate insulating film 103," and "a gate electrode 108." Ex. 1003 at ¶¶ [0068]-[0069], [0071].

1[b]: a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other;

115. Kobayashi also discloses the plurality of claimed interconnections. Kobayashi's "plurality of interconnections" are "auxiliary wiring elements 118 [that] are interconnected over the entire display region 10," and that project above the surface of "insulating layer 116" (which, as I have explained above, corresponds to the upper surface of the claimed "transistor array substrate." Ex. 1003 at ¶ [0088]. These projecting interconnections 118 are illustrated by Figure 7 of Kobayashi:

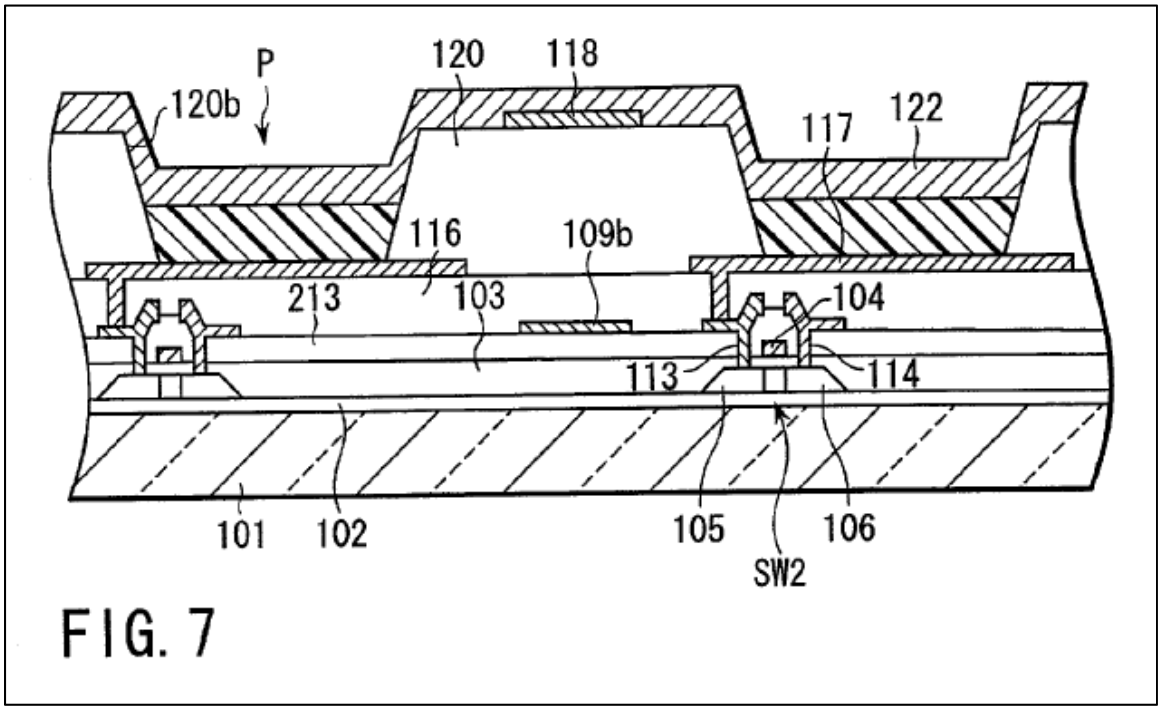


FIG. 7

116. The "auxiliary wiring elements 118" of Kobayashi are each "electrically connected to the second electrode 122," which lowers the resistance of that second electrode 122, preventing voltage drops across its surface and allowing the display screen of Kobayashi to present a uniform appearance. Ex. 1003 at ¶¶ [0062], [0083]. The functionality of Kobayashi's "auxiliary wiring elements 118" serves precisely the same purpose as the '338 patent's so-called "common interconnections"—as the '338 patent explains, each "common interconnection 91 reduce the sheet resistance of the cathode electrode[s]." Ex. 1001 at 14:8-19.

117. Also like the '338 patent, Kobayashi explains that its "auxiliary wiring elements 118" are formed on "partition walls 120," Ex. 1003 at ¶ [0088], like the '338 patent's common interconnections that are formed on top of "insulating line 61" as shown in Figure 6 of the '338 patent:

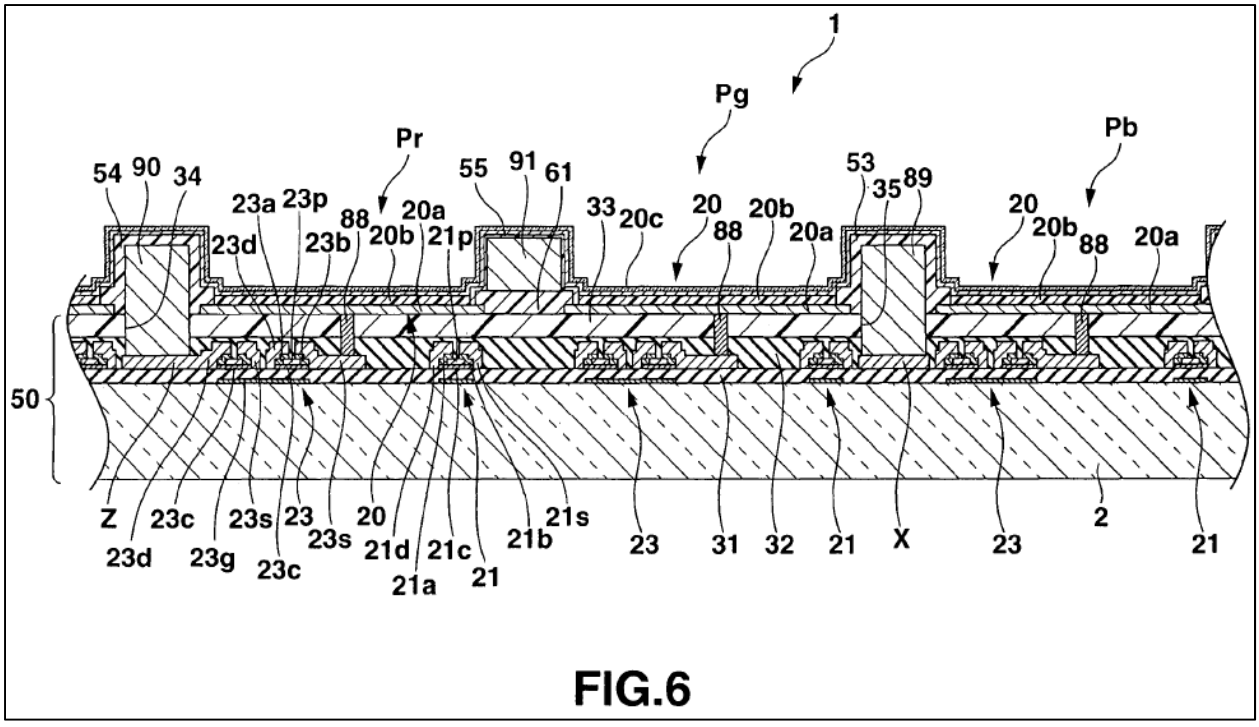


FIG.6

118. Kobayashi also describes how these "auxiliary wiring elements 118" that correspond to the claimed "interconnections" are arrayed in parallel to each other, disclosing that they are "disposed in a lattice shape," as stated in paragraph [0088] and as shown in Figure 1 of Kobayashi:

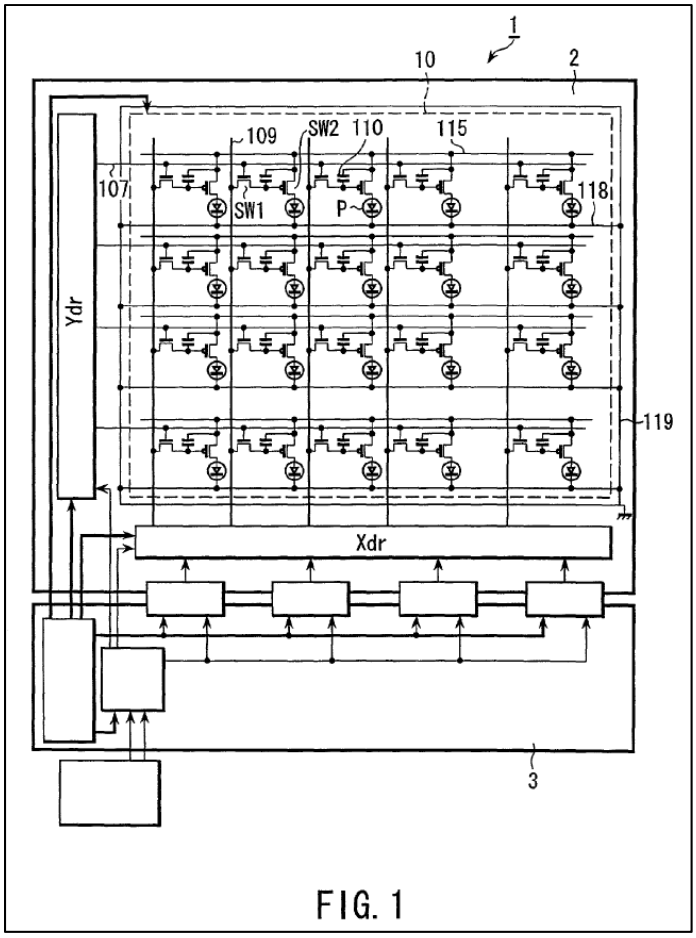


FIG. 1

119. Accordingly, a POSA would have recognized that Kobayashi disclosed this claim limitation.

1[c]: "a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate;"

120. Kobayashi discloses a plurality of pixel electrodes which are (a) arrayed between & along the interconnections, and (b) arrayed on the surface of the transistor array substrate. Specifically, this limitation corresponds to Kobayashi's "first electrodes 117," Ex. 1003 at ¶¶ [0057], [0092], as I explain further below.

"a plurality of pixel electrodes for the plurality of pixels, respectively"

121. A POSA would have recognized that Kobayashi disclosed this claim limitation—Kobayashi explains that each of its organic EL display element P comprises a first electrode 117," Ex. 1003 at ¶ [0044], and that each first electrode 117 "functions as the anode of the organic EL display element," Ex. 1003 at ¶ [0051].

"the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate"

122. A POSA would have also recognized that Kobayashi disclosed this claim element. Kobayashi explains that its "auxiliary wiring elements 118" that correspond to the claimed "interconnections" "are formed in a lattice shape so as to surround the first electrode 117 of each display element P" (which, as I have explained above, correspond to the claimed "pixel electrodes"). Ex. 1003 at ¶ [0046]. In other words, Kobayashi discloses that the "interconnections" "surround the pixels of all display elements P," Ex. 1003 at ¶ [0090], meaning that the pixel electrodes of those pixels will be arrayed between and along those interconnections, as shown in Fig. 1 of Kobayashi:

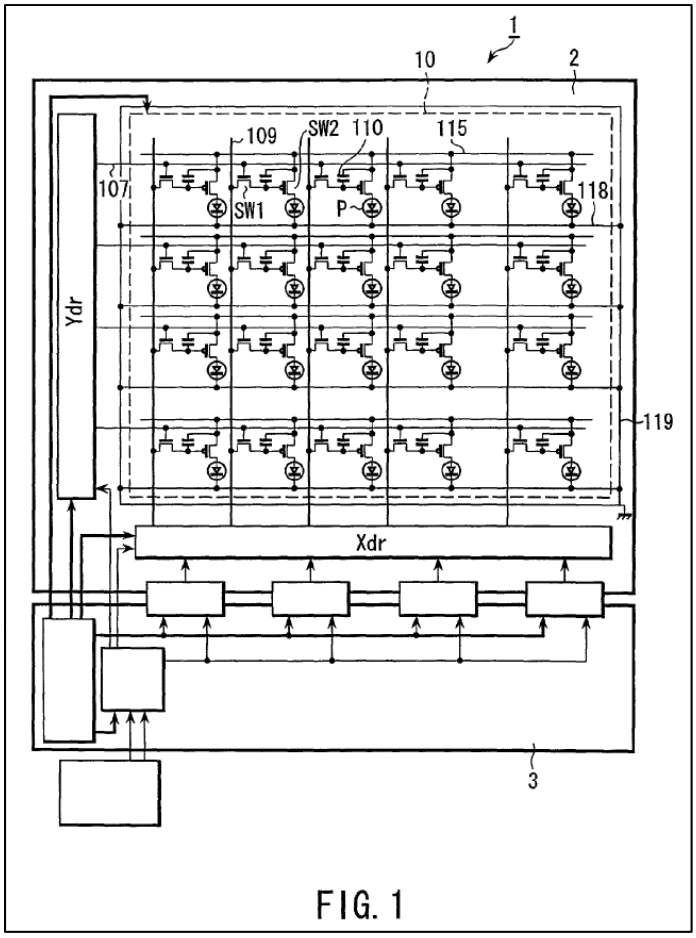


FIG. 1

123. Kobayashi also describes how the "first electrodes 117" that correspond to the claimed "pixel electrodes" are "disposed on" the surface of "insulating layer 116," which as I have explained above corresponds to the top surface of the claimed transistor array substrate. Ex. 1003 at ¶ [0074]. This is illustrated by Figure 7 of Kobayashi:

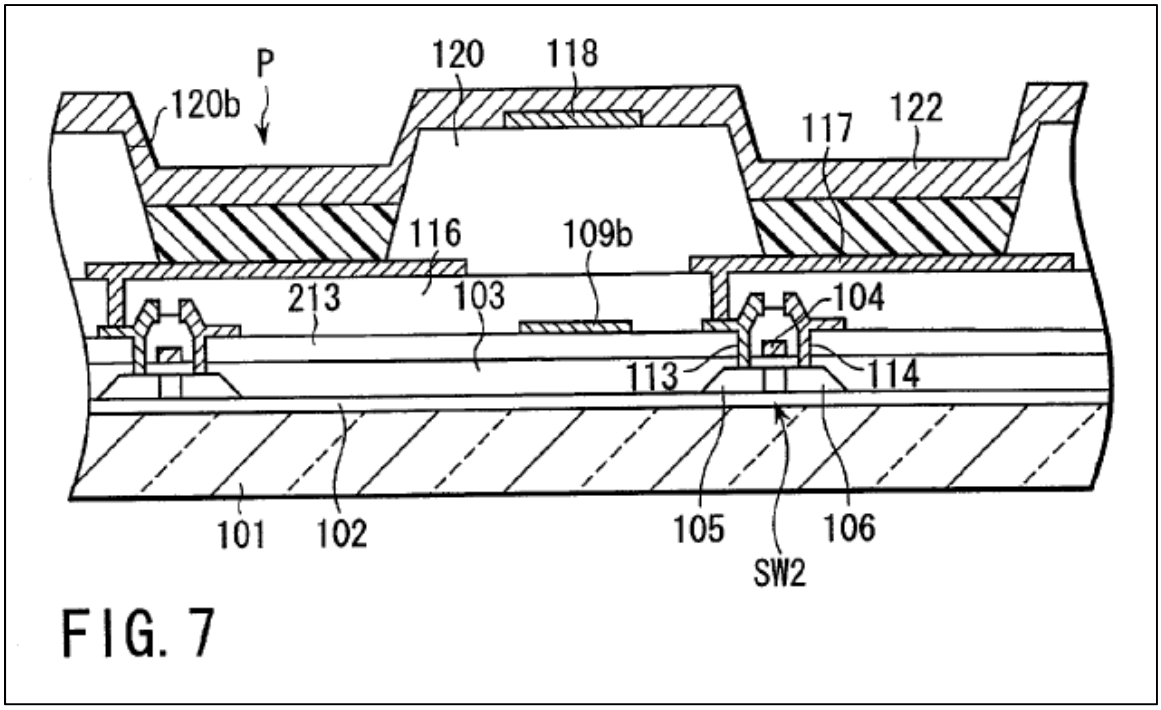


FIG. 7

124. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

1[d]: a plurality of light-emitting layers formed on the pixel electrodes, respectively; and

125. Kobayashi also discloses the claimed "plurality of light-emitting layers." Specifically, Kobayashi discloses that "organic light-emission layers 121" are "formed on" (or, in other words, "disposed on") each "first electrode 117" (which, as discussed above, correspond to the claimed pixel electrodes) in each "display element P." Ex. 1003 at ¶¶ [0044], [0079]-[0080], [0092]. This is depicted in Figure 7 of Kobayashi, above, although the diagram appears to inadvertently omit label 121 for the OLED element between elements 117 (anode) and 122 (cathode).

126. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

1[e]: a counter electrode which is stacked on the light-emitting layers,

127. Kobayashi discloses the claimed "counter electrode." More specifically, Kobayashi describes a "second electrode 122" which "is provided commonly for all the display elements P," Ex. 1003 at ¶ [0057], and that is a ""cathode" "of the organic EL display element," Ex. 1003 at ¶ [0051]. This cathode/second electrode 122 is formed on organic-light emission layer 121, as illustrated in Figure 7 of Kobayashi, Ex. 1003 at ¶¶ [0044], [0080]:

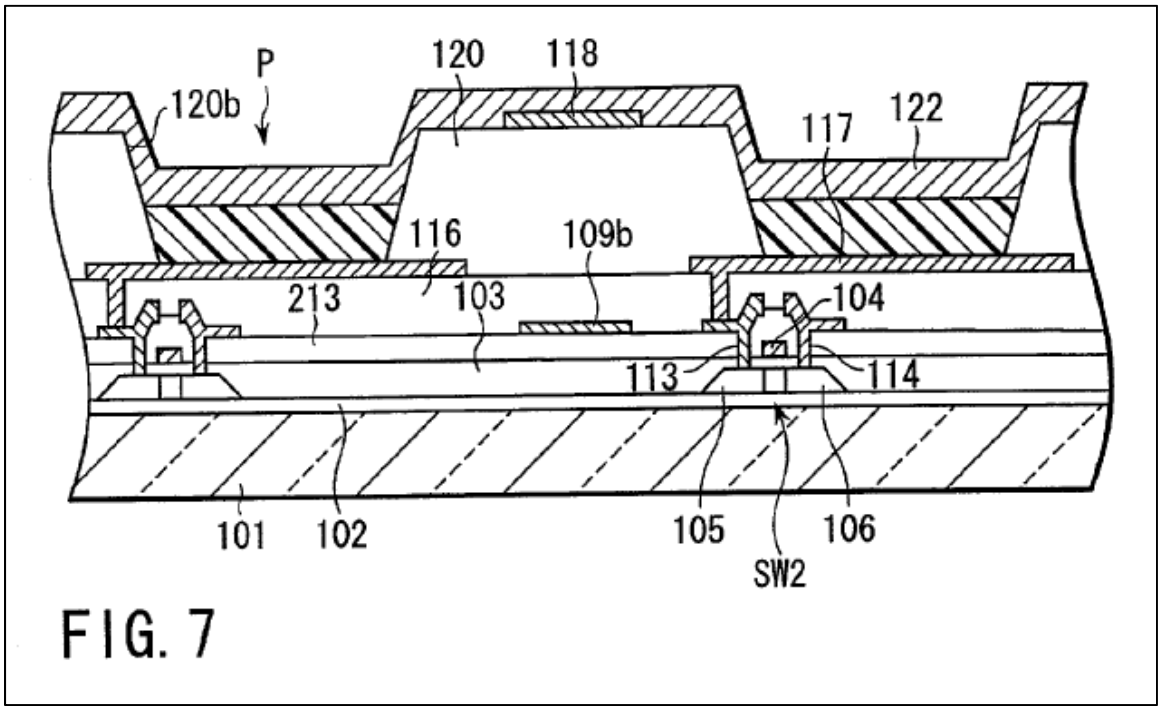


FIG. 7

128. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

1[f]: wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

129. A POSA would have recognized that this limitation would have been obvious in view of the combination of Kobayashi and Shirasaki.

130. Kobayashi discloses, for each pixel, a plurality of transistors that include: (a) a driving transistor, one of the source and the drain of which is connected to the pixel electrode, and (b) a switch transistor which makes a write current flow between the drain and the source of the driving transistor.

131. In particular, Kobayashi describes a "driving control element SW2" for each pixel, which corresponds to the claimed "driving transistor." Ex. 1003 at ¶ [0043]. Kobayashi explains that the source of this "driving control element SW2" is connected to "the first electrode 117 of display element P" (which, as I have explained above, corresponds to the claimed "pixel electrode"). Ex. 1003 at ¶ [0074].

132. Kobayashi also describes a "switching element SW1" for each pixel, which corresponds to the claimed "switching transistor." Ex. 1003 at ¶ [0043]. The source of each switching element SW1 is connected to the gate of driving element

SW2 for each pixel, and therefore controls whether a current flows between the drain and the source of the driving transistor SW2, as Figure 1 of Kobayashi shows:

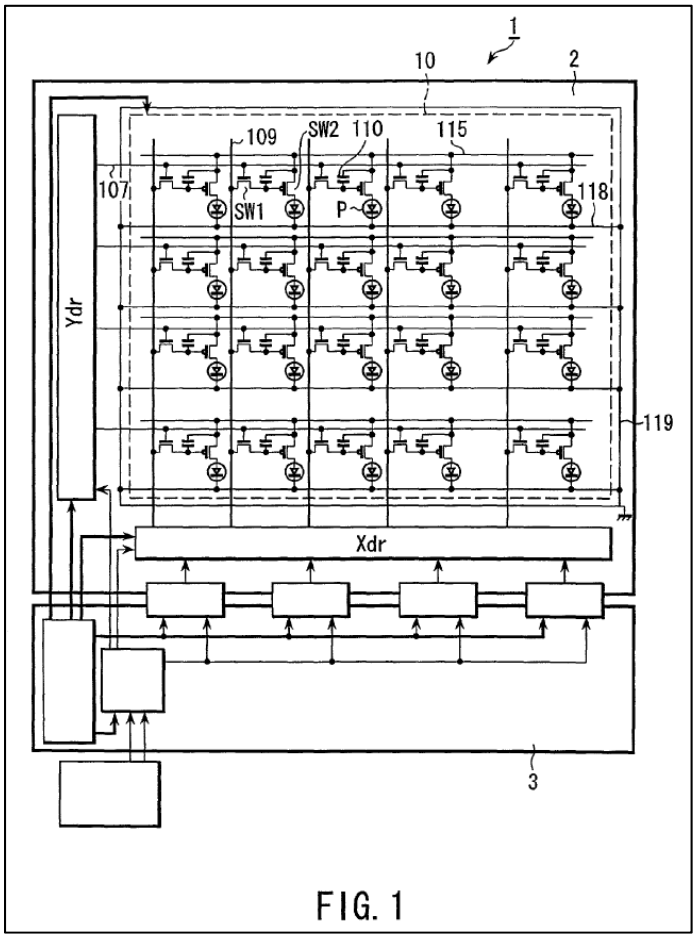


FIG. 1

133. However, Kobayashi does not disclose the third transistor required by this claim limitation: the "holding transistor" which "holds a voltage between the gate and source of the driving transistor in a light emission period."

134. The addition of the claimed "holding transistor" to Kobayashi's pixel circuit, however, would have been obvious to a POSA in September 2004, based on Shirasaki, which not only disclosed the exact same three-transistor structure claimed by the '338 patent, but explained why a POSA would have been motivated to replace

Kobayashi's two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit.

135. First, regarding the disclosure of Shirasaki, Shirasaki's figures illustrate the same three-transistor pixel circuit that was later used by Casio again in the figures for the '338 patent. I note that transistor 11 in Fig. 5B of Shirasaki corresponds to "switch transistor 21" in Figure 2 of the '338 patent, transistor 12 in Figure 5B of Shirasaki corresponds to "driving transistor" 23 in Figure 2 of the '338 patent, and transistor 10 in Shirasaki corresponds to "holding transistor" 22 in Figure 2 of the '338 patent:

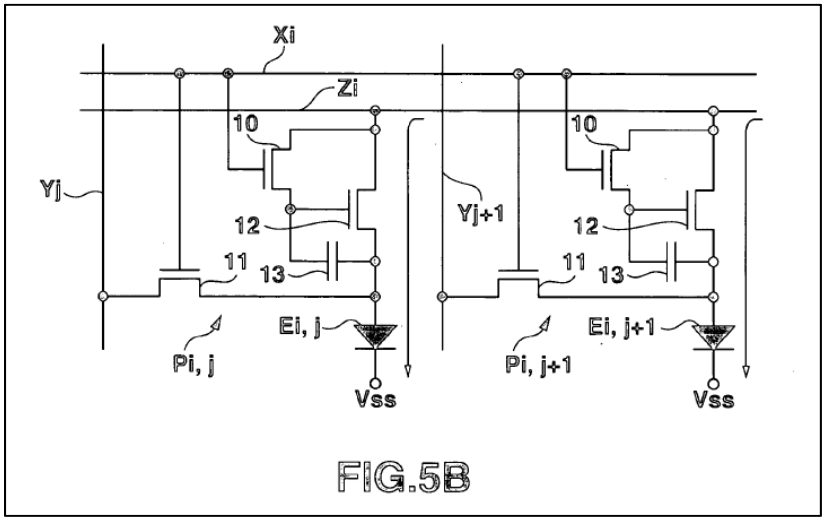


FIG.5B

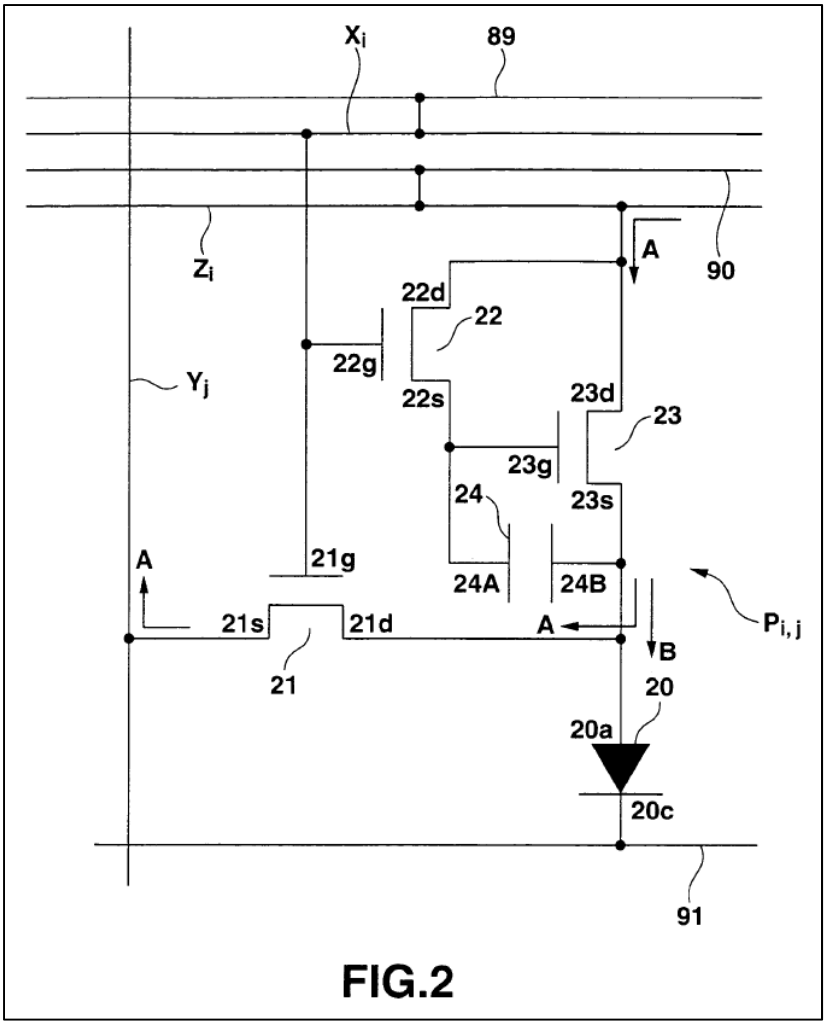


FIG.2

136. Further, as I have explained above, Kobayashi and Shirasaki each disclose AMOLED display panels and the TFT pixel circuits that are found in each pixel of those AMOLED display panels. And as I also note above, Shirasaki not only discloses the three-transistor pixel circuit structure claimed in the '338 patent, but explains why a POSA would have been motivated to replace Kobayashi's two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit.

137. Shirasaki explains that in a "conventional light emitting element display," where "two transistors are formed in one pixel," Ex. 1004 at ¶¶ [0003], [0004], that:

> The channel resistances of the transistors 103 and 104 depend upon the ambient temperature and change after a long-term operation. Therefore, it is difficult to display images with a desired luminance tone for long time periods.
>
> . . .
>
> This varies the magnitudes of the drain-source currents of the transistors 104 in the individual pixels, resulting in variations in the display characteristics of the individual pixels in a single panel. As a consequence, no accurate tone control can be performed. Accordingly, variations in the characteristics of the transistor 104 of each pixel must fall within a range required to control the tone of each pixel. However, as the resolution of an EL element increases, it becomes more difficult to make the characteristics of the transistors 104 of the individual pixels uniform.
>
> Ex. 1004 at ¶ [0007].

138. Shirasaki goes on to explain the multiple benefits that result when that two-transistor pixel circuit structure are replaced with its disclosed three-transistor pixel circuit structure:

> In the display panel having the above [three-transistor] arrangement, the current memory circuit stores the current data corresponding to the current value of the memory current flowing during the selection period. Accordingly, the display current having a current value substantially equal to the memory current can be supplied to the optical

> element. Current control is thus performed by the current values, not by voltage values. This suppresses the influence of variations in the voltage-current characteristic of the control system and allows the optical element to stably display images with desired luminance.
>
> Ex. 1004 at ¶ [0018].

139. Shirasaki also specifically states that "one advantage of the present invention is that pixels stably display image with desired luminance in a display panel." Ex. 1004 at ¶ [0011]. I note that while Kobayashi discloses a "capacitor 110 for holding a video signal voltage," Ex. 1003 at ¶ [0043], a POSA would have recognized that this capacitor would not have provided the same advantages as Shirasaki's "holding transistor"—as evidenced by the fact that the pixel circuits of both Shirasaki as well as of the '338 patent still include a capacitor in addition to the claimed "driving," "switch," and "holding" transistors in their pixel circuits.

140. Furthermore, Shirasaki explains why a three-transistor structure should be chosen instead of a pixel circuit with four or more transistors per pixel, Ex. 1004 at ¶ [0009], stating that in its three-transistor pixel circuit structure "the display area per pixel of a display panel is increased" and therefore "the apparent brightness improves accordingly" (in comparison to a four-transistor (or more) pixel circuit structure), Ex. 1004 at ¶¶ [0012], [0020]. Shirasaki also explains that the three-transistor circuit will have a comparatively "low voltage and consequently low power consumption driving." Ex. 1004 at ¶ [0019].

141. Accordingly, a POSA would have recognized the advantages provided by Shirasaki's three-transistor pixel circuit structure, and would have been motivated to modify Kobayashi's AMOLED display panel by replacing its two-transistor pixel circuit with the three-transistor pixel circuit disclosed by Shirasaki.

142. Furthermore, it would have been straightforward for a POSA to modify Kobayashi in the manner I have described above, and a POSA would have readily expected success in (and predictable results from) making this modification for several different reasons.

143. First, as I have discussed above, Shirasaki discloses that its three-transistor pixel circuit was designed and meant to replace the two-transistor pixel circuits found in "conventional" AMOLED devices such as Kobayashi, Ex. 1004 at ¶¶ [0002]-[0008], [0013]-[0019], and thus a POSA would have readily expected success in modifying Kobayashi in this manner. This expectation of success would have been further bolstered by the fact that both Kobayashi and Shirasaki are directed to AMOLED display panels with thin-film transistor circuits. Ex. 1003 at ¶ [0002], Ex. 1004 at ¶¶ [0041], [0043].

144. Furthermore, as I have discussed at length above, Kobayashi explains how all of the thin-film transistors that make up its pixel circuits (and the wiring of those pixel circuits) are contained "under the insulating layer 116" (corresponding

to the "planarization film 33" of the '338 patent), and that the OLED "display element[s] P" are "formed over" that insulating layer 116. Ex. 1003 at ¶ [0060].

145. Accordingly, a POSA would have recognized that Kobayashi's two-transistor pixel circuit could be replaced with Shirasaki's three-transistor pixel circuit without altering the layer structure of any of the layers above Kobayashi's "insulating layer 116" (which, as I have discussed above, corresponds to the upper surface of the claimed "transistor array substrate"). I note that Kobayashi itself explains that the light emission of its OLED elements (located on top of insulating layer 116) occurs "irrespective of circuits such as TFTs" that are located "under the insulating layer 116." Ex. 1003 at ¶¶ [0004], [0060].

146. More specifically, while modifying Kobayashi to replace its two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit would have necessitated changing the photomasks used to fabricate the TFT array in Kobayashi and relocating the contact holes through Kobayashi's "insulating layer 116," these were known and routine manufacturing steps to a POSA at the time that would have been involved during the fabrication of any AMOLED device. I note that Childs, for example, repeatedly described how "photolithographic masking and etching techniques" such as this were already "known" to those of skill in the art by the September 2004 timeframe. Ex. 1005 at 14:29-15:2, 15:25-28, 16:8-10.

b. Dependent Claim 2

A panel according to claim 1, wherein said plurality of interconnections include at least one of a feed interconnection connected to the other of the source and the drain of at least one of the driving transistors, a select interconnection which selects at least one of the switch transistors, and a common interconnection connected to the counter electrode.

147. In my opinion, based on the language of this claim and the disclosure of the '338 patent, a POSA would have understood this claim to require that the claimed plurality of interconnections include at least one of the three types of interconnections described in the claim ("feed," "select," or "common") (as opposed to requiring at least one of each of the three types of interconnections, as claim 4 requires).

148. Further, a POSA would also have appreciated that Kobayashi discloses this claim limitation. Kobayashi describes how its "auxiliary wiring elements 118" are "electrically connected to the second electrode 122," and that this serves to lower the resistance of the "second electrode 122" (the cathode of the OLED display element) to promote a uniform appearance of Kobayashi's display screen and prevent voltage drops. Ex. 1003 at ¶¶ [0062], [0083]. This disclosure from Kobayashi corresponds to the '338 patent's disclosure explaining how the "common interconnection 91 reduce[s] the sheet resistance of the cathode electrode" in the '338 patent. Ex. 1001 at 14:8-19.

c. Dependent Claim 5

A panel according to claim 1, wherein said plurality of pixels include a red pixel, a green pixel, and a blue pixel.

149. Kobayashi discloses that its plurality of pixels includes a red pixel, a green pixel, and a blue pixel. Kobayashi discloses that the "organic EL panel 2 comprises three kinds of display elements P, which respectively emit red, green, and blue light." Ex. 1003 at ¶ [0041]. Kobayashi also repeatedly discusses the different colors of its display elements P (i.e., pixels). Ex. 1003 at ¶¶ [0044], [0056]. Furthermore, Kobayashi explains that "organic light-emission materials corresponding to red (R), green (G), and blue (B) are successively jetted out by an ink-jet method," and, therefore, "organic light-emission layers 121 of the respective colors are selectively formed." Ex. 1003 at ¶ [0079].

150. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

d. Dependent Claim 6

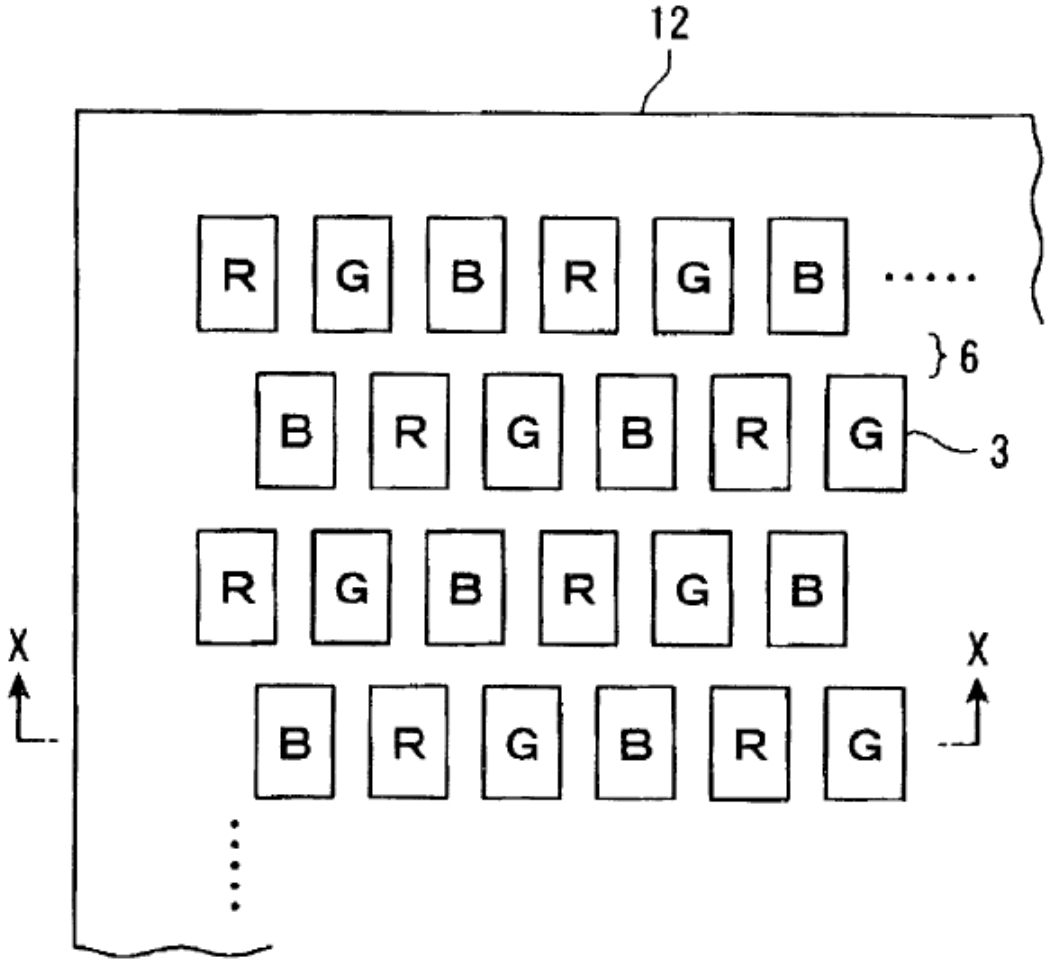
A panel according to claim 5, wherein said plurality of pixels comprises a plurality of sets each including the red pixel, the green pixel, and the blue pixel arrayed in an arbitrary order.

151. Kobayashi similarly discloses that the plurality of pixels comprises a plurality of sets each including the red pixel, the green, pixel, and the blue pixel arrayed in an arbitrary order. As I note above, Kobayashi discloses that the "organic EL panel 2 comprises three kinds of display elements P, which respectively emit red,

green, and blue light." Ex. 1003 at ¶ [0041]. Kobayashi also repeatedly discusses the different colors of its display elements P (i.e., pixels). Ex. 1003 at ¶¶ [0044], [0056]. Furthermore, Kobayashi explains that "organic light-emission materials corresponding to red (R), green (G), and blue (B) are successively jetted out by an ink-jet method," and, therefore, "organic light-emission layers 121 of the respective colors are selectively formed." Ex. 1003 at ¶ [0079].

152. Further, a POSA would have recognized that these red, green, and blue pixels would be arrayed in an arbitrary order. Such RGB displays were well known to those of skill in the AMOLED art at the time, and contemporary prior art such as Nakamura, for example, commonly disclosed that such displays would be arranged in an arbitrary order, as illustrated by Figure 33A of Nakamura (Ex. 1007):

FIG. 33A



153. Accordingly, a POSA would have appreciated that Kobayashi disclosed this claim limitation.

e. Dependent Claim 9

A panel according to claim 1, wherein at least one of the interconnections has a resistivity of 2.1 to 9.6 μΩcm.

154. Kobayashi discloses that its interconnections have a resistivity falling within this claimed range. Specifically, Kobayashi explains that "it is preferable, in particular, that the auxiliary wiring element be formed of a conductive material with a resistivity of $1x10^{-6}$ Ωcm to $6x10^{-6}$ Ωcm." Ex. 1003 at ¶ [0049]. Kobayashi further provides a specific example in which the "resistivity of the auxiliary wiring element 118 . . . is about 3 μΩcm." Ex. 1003 at ¶ [0089]. And Figure 4 of Kobayashi provides a table with "the electrical resistivity (μΩcm) of typical metal materials chosen for the auxiliary wiring element 118, including a number of materials having resistivities in the claimed range," Ex. 1003 at ¶ [0049]:

FIG. 4

METAL MATERIAL	ELECTRICAL RESISTIVITY (μΩcm)	TRANSPARENT CONDUCTIVE MATERIAL	ELECTRICAL RESISTIVITY (μΩcm)
Ag	1.6	ITO	100～1000
Cu	1.7	IZO	100～1000
APC alloy	2.2		
Au	2.4		
Al	3.0		
Al-Nd alloy	4.7		
Ti	5.0		
Mo	5.6		
W	5.6		

155. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

f. Dependent Claim 10

A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer that is different from a layer forming the source and the drain of each of the transistors and a layer forming the gate of the transistors.

156. Kobayashi discloses that its plurality of interconnections are formed from a conductive layer different than the layers forming the source, gate, and drain of the transistors, as recited above. Kobayashi explains that its "auxiliary wiring elements 118" (which, as I have explained above, correspond to the claimed "plurality of interconnections") are made out of "metal materials." Ex. 1003 at ¶ [0049]. In contrast, the source, drain, and gate of Kobayashi's transistors are formed from polysilicon. Ex. 1003 at ¶¶ [0065]-[0069]. Further, as depicted by Figure 7 of Kobayashi, these "auxiliary wiring elements 118" are clearly formed from a conductive layer that is different than the layer forming the source and drain 105 and 106 of each of transistors SW2, or the layer forming the gate 104 of transistors SW2, all of which are formed *under* insulating layer 116:

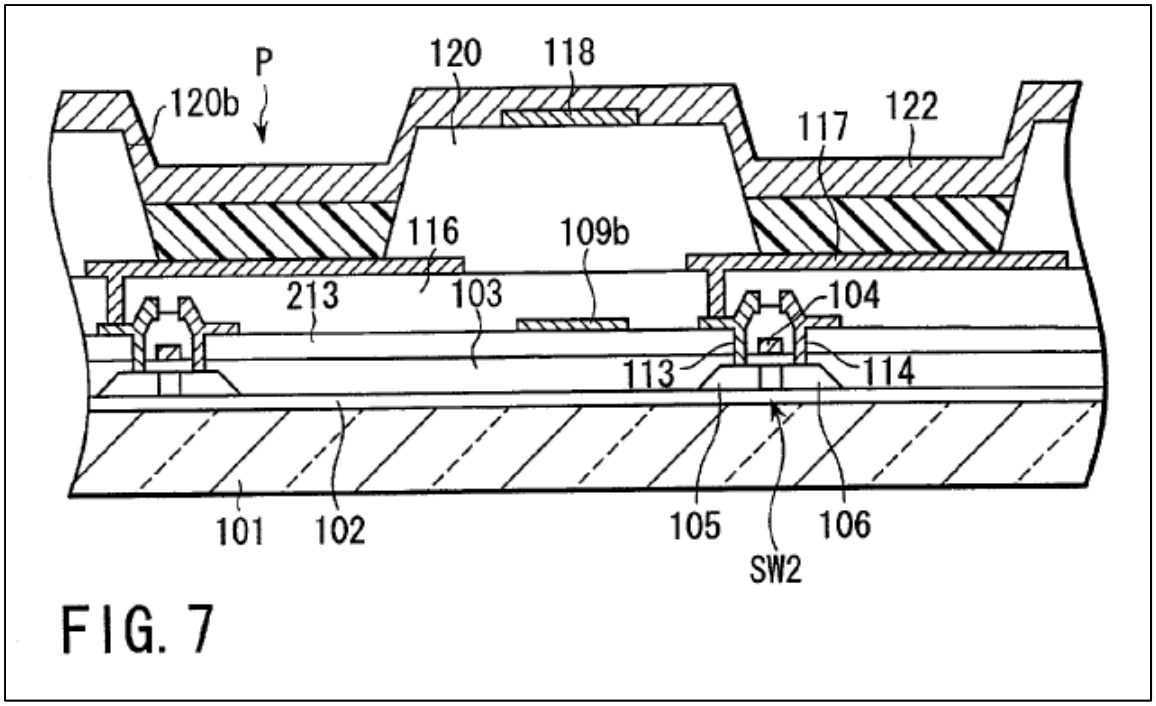


FIG. 7

157. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

g. Dependent Claim 11

A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer different from a layer forming the pixel electrodes.

158. Kobayashi discloses that its plurality of interconnections are formed from a conductive layer different than the layer forming the pixel electrodes. As illustrated by Figure 7, Kobayashi's "auxiliary wiring elements 118" (which, as I have explained, correspond to the claimed "plurality of interconnections") are formed on top of the insulating material of "partition walls 120," with those partition walls 120 in turn being formed on top of the "first electrodes 117" (which correspond to the claimed "pixel electrodes"), Ex. 1003 at ¶ [0092]:

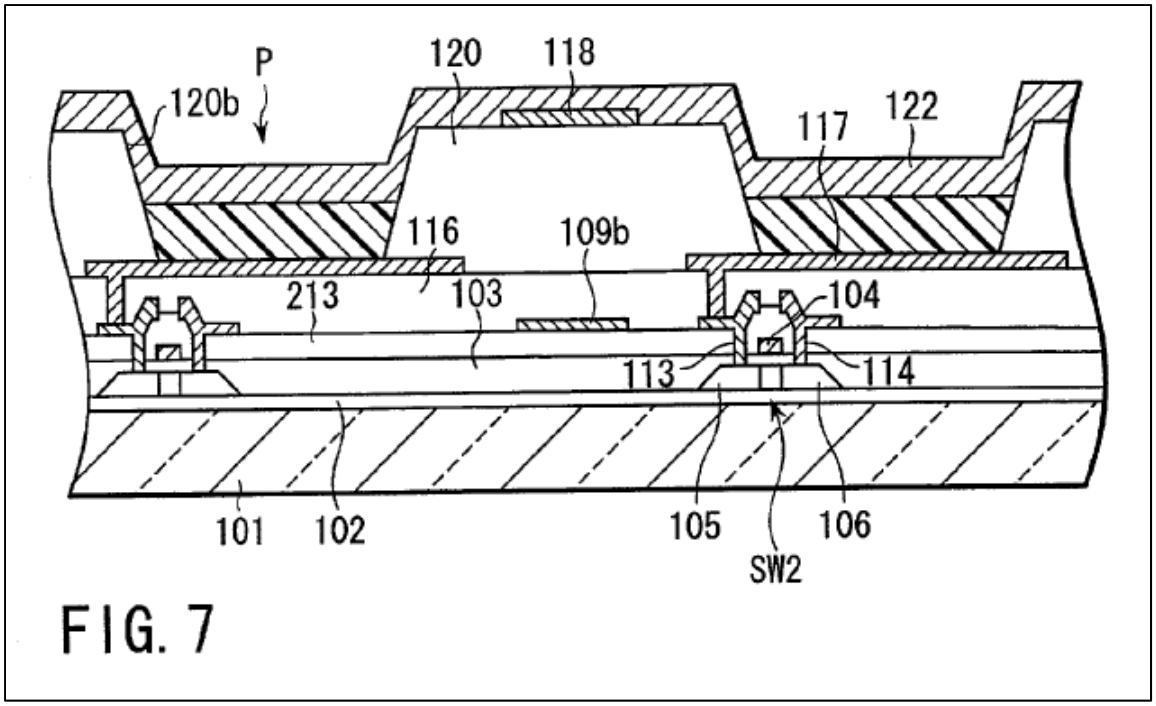


FIG. 7

159. Accordingly, a POSA would have appreciated that Kobayashi discloses this claim limitation.

X. THE COMBINATION OF CHILDS AND SHIRASAKI (CLAIMS 1-3, 5-13)

160. Childs and Shirasaki each come from the same technological field: the structure of an AMOLED display panel. Accordingly, in this particular case, a POSA would have looked to the disclosures of these references together when designing an AMOLED display panel.

161. The particular combinations of Childs and Shirasaki's features that a POSA would have had reason to make, and his or her reasons for making these combinations, are discussed in further detail below. However, in summary, my analysis below concludes that a POSA would have been motivated to and readily

capable of combining the features in Childs and Shirasaki to arrive at what is claimed in the ’338 patent based on the disclosures in the prior art and a POSA’s knowledge of the art in the September 2004 timeframe of the ’338 patent.

a. Independent Claim 1

1[preamble]: A display panel comprising:

162. Childs discloses the claimed display panel. Specifically, Childs discloses an “active-matrix electroluminescent display (AMELD) device.” Ex. 1005 at 6:23-25. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

1[a]: a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain;

163. A POSA would have recognized that Childs discloses the claimed “transistor array substrate.”

164. As I have explained above in my discussion of the proper claim construction for this claim element, a POSA, in accordance with the disclosure and claims of the ’338 patent, would have understood this claim element to encompass a layered structure from a bottom substrate through a topmost insulating layer, upon which pixel electrodes are formed. I noted above, for example, that the ’338 patent’s specification states that “the layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50,” Ex. 1001 at 10:42-47,

and refers to "the upper surface of the planarization film 33, i.e., the upper surface of the transistor array substrate 50," Ex. 1001 at 11:50-55.

165. Childs describes a layered structure that extends from "insulating glass base 10" through the uppermost surface of "planar insulating layer 12" (including "insulating layers 11, 2, and 8), which Childs refers to in its entirety as "circuit substrate 100," Ex. 1005 at 7:31-8:27, as illustrated by Fig. 2 of Childs, and as described in 14:30-32 of Childs, which refers to "the thin-film circuit substrate 100 with its upper planar insulating layer 12":

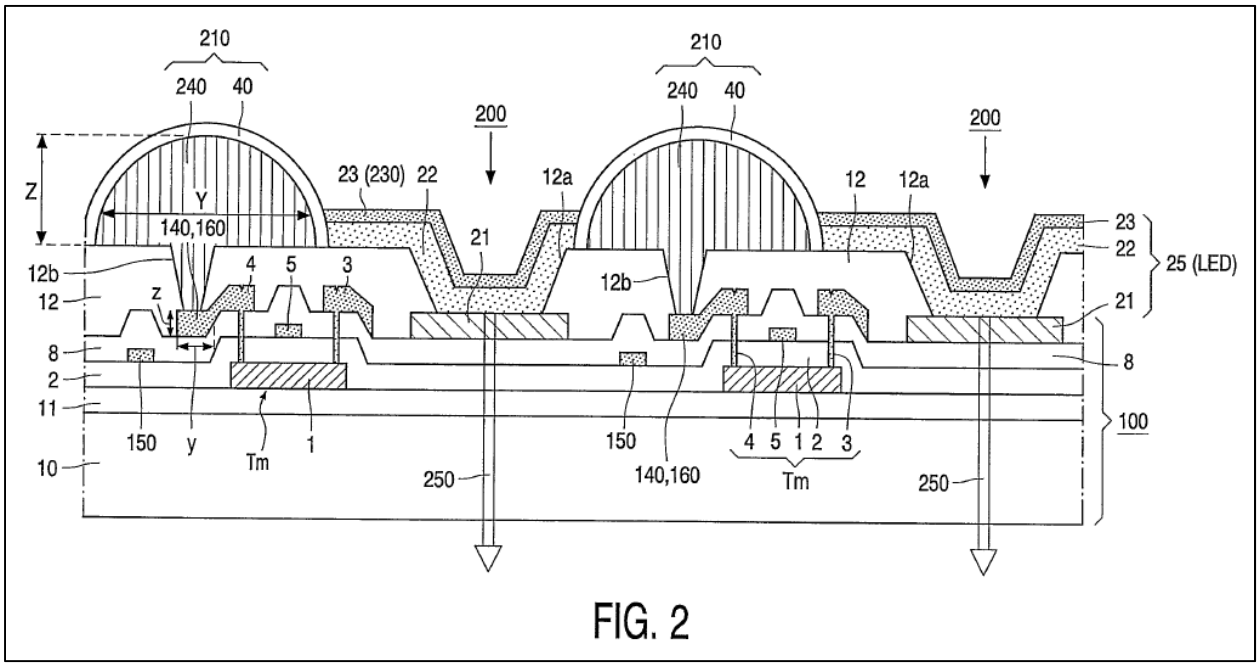


FIG. 2

166. A POSA would have recognized that Childs' layered "circuit substrate 100" structure includes a "transistor array substrate" as claimed by the '338 patent.

167. Furthermore, a POSA would also have recognized that Childs' layered "circuit substrate 100" structure additionally: (a) includes a plurality of pixels and

(b) comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain, as claim 1 requires:

"includes a plurality of pixels"

168. Childs explains that its "active-matrix electroluminescent display (AMELD) device . . . comprises an array of pixels 200 on a circuit substrate 100," where there are "[p]hysical barriers 210 . . . between at least some of the neighbouring pixels." Ex. 1005 at 6:23-27. These pixels 200 are illustrated in Figure 2 of Childs:

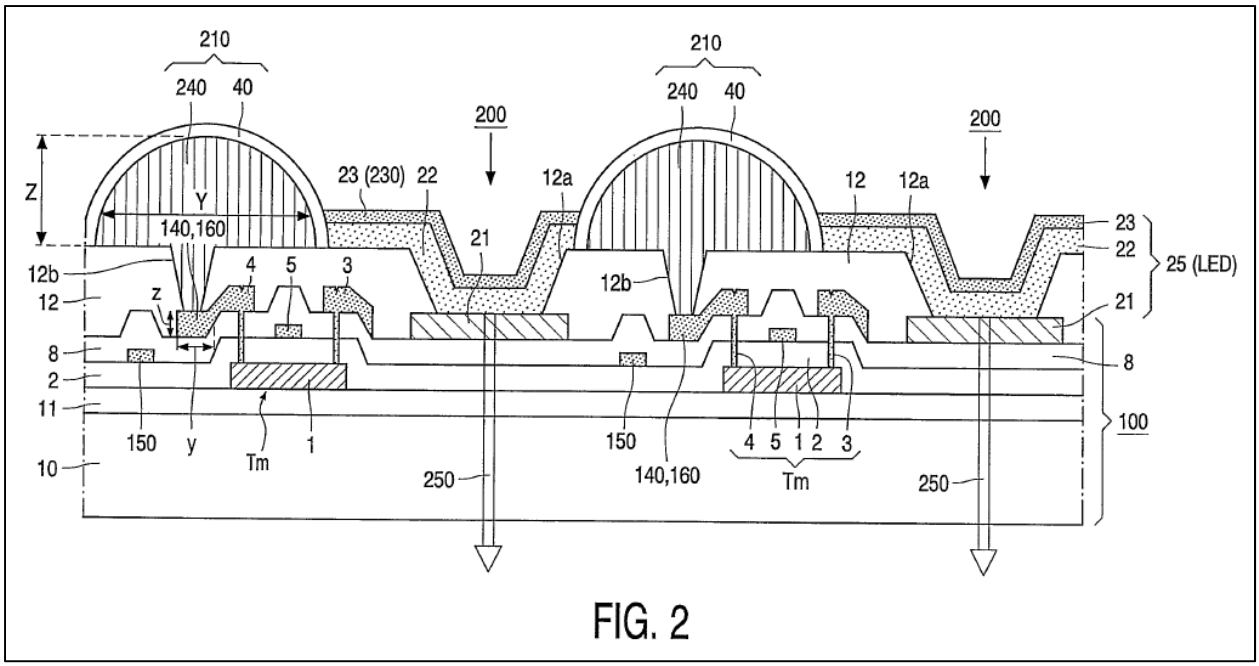


FIG. 2

"comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain"

169. Childs also discloses that its "circuit substrate 100" comprises a plurality of transistors for each pixel. As Figure 1 of Childs illustrates, each "pixel

200 comprises" both a "drive TFT T1" as well as an "addressing TFT T2." Ex. 1005 at 7:10-30. This two-transistor pixel circuit structure is illustrated by Figure 1 of Childs:

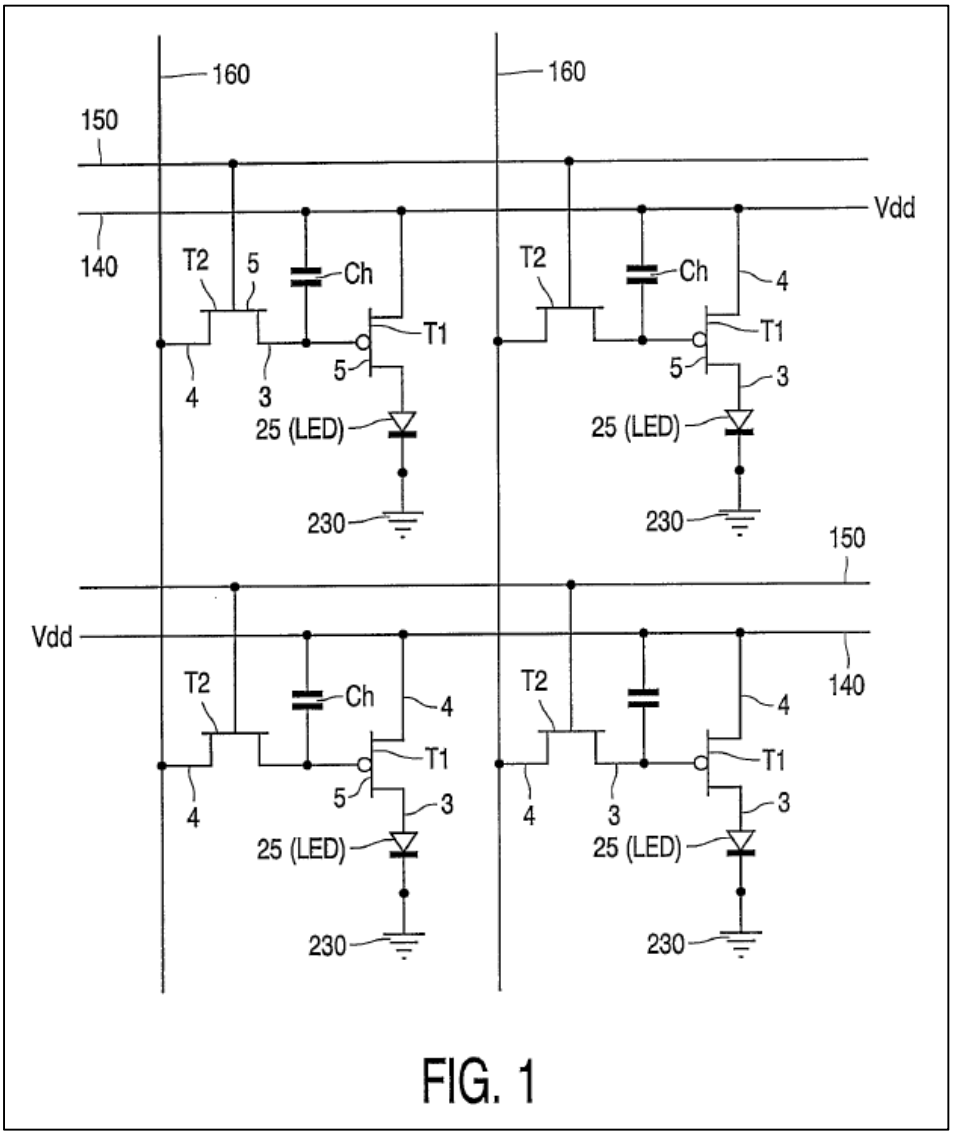


FIG. 1

170. Further, as illustrated by Figure 2 of Childs, each of these transistors T1 and T2 ("Tm") are found within "circuit substrate 100," and each is made up of an "active semiconductor layer 1" with "source and drain regions" (which are

connected to "electrodes 3 and 4"), a "gate electrode 5," and "a gate dielectric layer 2" (the claimed "gate insulating film"), Ex. 1005 at 8:3-15:

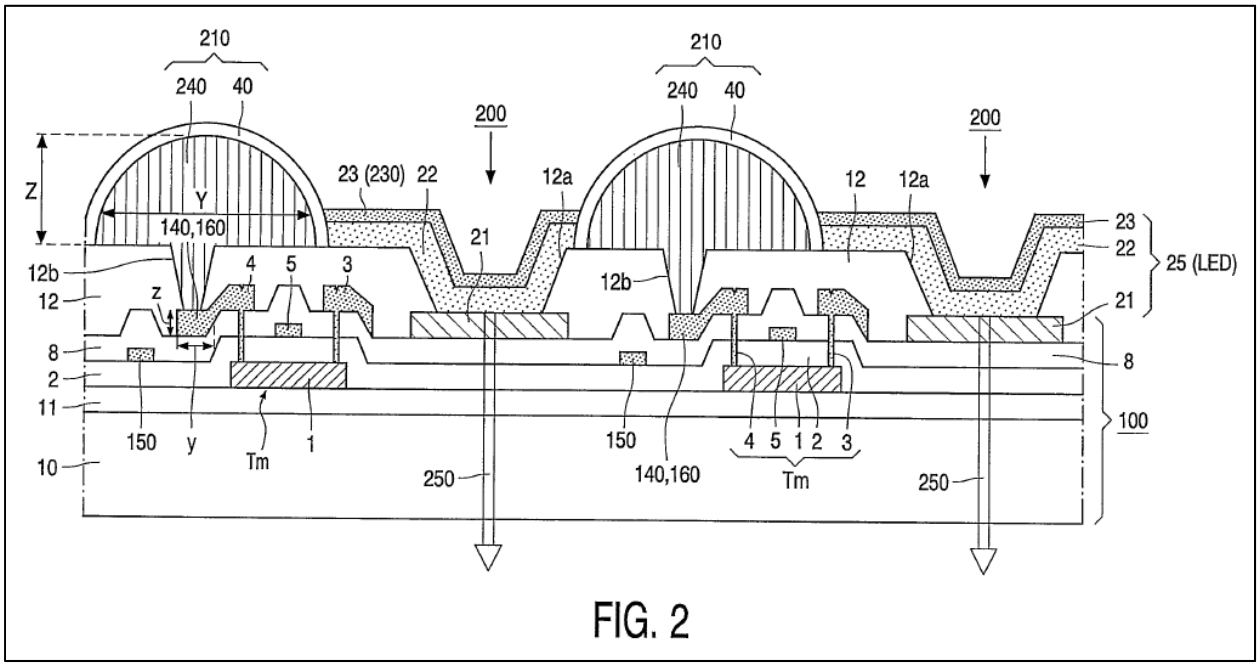


FIG. 2

171. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

1[b]: a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other;

172. Childs discloses the claimed "plurality of interconnections" as well. Specifically, Childs discloses that the "physical barriers 210" in its OLED structure "are constructed with conductive barrier material 240 that is used as an interconnection," Ex. 1005 at 6:25-29, and that these interconnections are "deposited on the insulating layer 12," Ex. 1005 at 15:9-23. Accordingly, these "interconnections" project from the surface of the circuit substrate 100 (in other

words, project from the surface of the claimed "transistor array substrate") and are arrayed in parallel to each of the other interconnections, as depicted by elements 240 in Figure 2 of Childs:

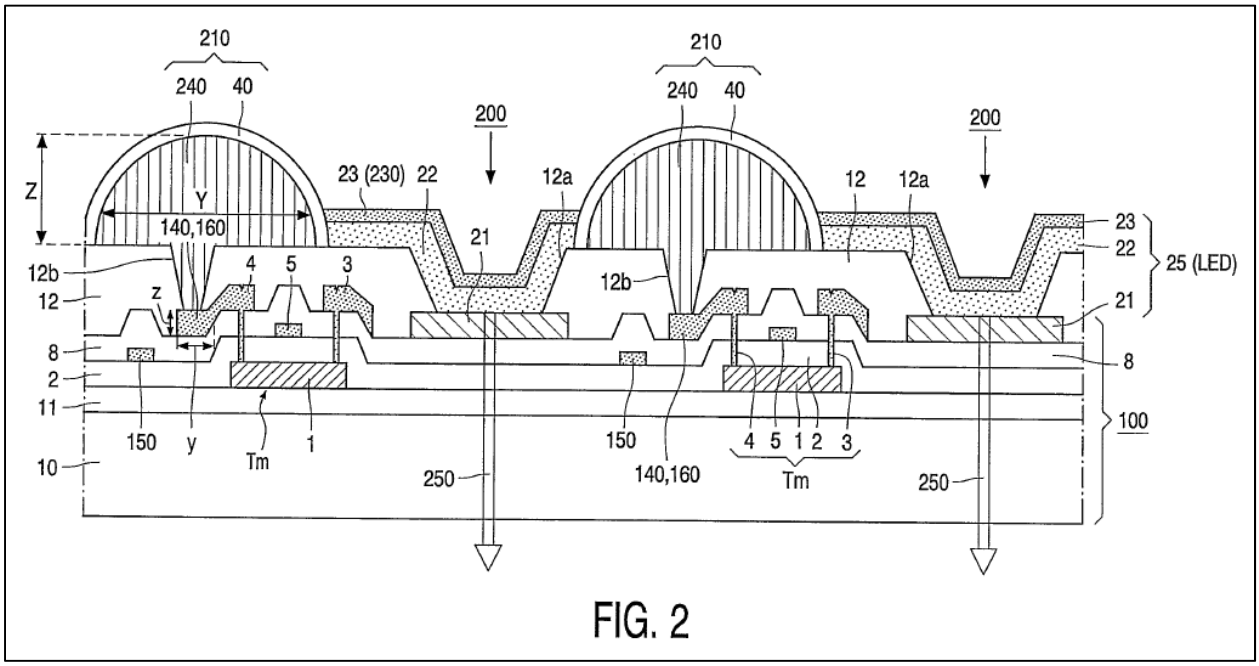


FIG. 2

173. These "conductive barrier[s] 240" are "connected to and/or from one or more circuit elements of the circuit substrate 100," where Childs specifically discloses "supply line 140," "addressing line 150, and/or "signal line 160," as examples of such circuit elements. Ex. 1005 at 9:20-29. Childs explains that by these circuit elements being electrically connected to these interconnections, their "line resistance can be significantly reduced by using the conductive material 240 to replace or back up the conductor line 150 of the circuit substrate." Ex. 1005 at 10:25-27. Childs further notes that by arranging the conductive barriers 240 in parallel, they can "separate and prevent overflow . . . between the respective areas of the

individual pixels 200 . . . during the provision of [electroluminescent] polymer layers 22." Ex. 1005 at 9:3-11.

174. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

1[c]: "a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate;"

175. Childs discloses a plurality of pixel electrodes. Specifically, this claim limitation corresponds to Childs' "lower electrode 21" that serves as an anode for each pixel, Ex. 1005 at 8:16-27, as I explain further below.

"a plurality of pixel electrodes for the plurality of pixels, respectively"

176. A POSA would have recognized that Childs disclosed the claimed "plurality of pixel electrodes for the plurality of pixels." Childs discloses "lower electrode[s] 21" for each pixel, Ex. 1005 at 8:16-27, which correspond to the claimed "plurality of pixel electrodes."

"the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate"

177. A POSA would also have found this claim element to be obvious in view of the disclosure of Childs. Figure 2 of Childs illustrates how each of its lower electrodes 21 is arrayed along conductive barrier 240 and between conductive

barriers 240 (which, as I have explained above, correspond to the claimed "interconnections"):

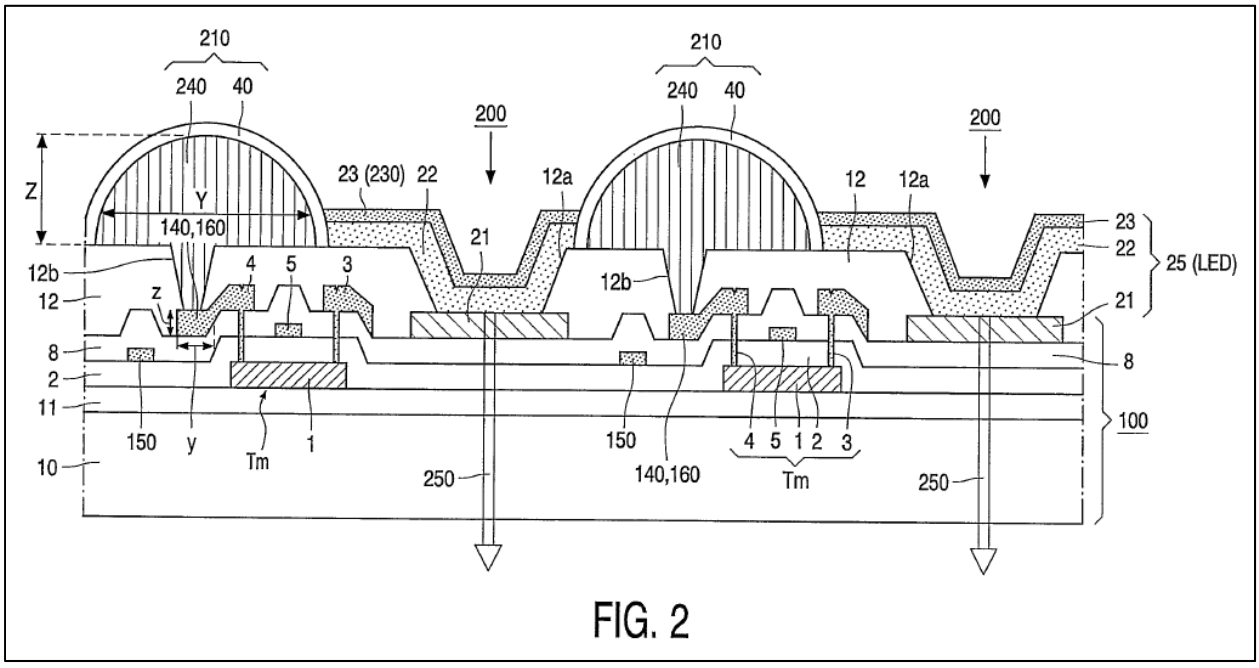


FIG. 2

178. Childs explains that each of these lower electrodes 21 is formed on top of insulating layer 8, with the "upper planar insulating layer 12" of the "circuit substrate 100" etched to create "connection windows 12a" (in other words, trenches) that expose the lower electrodes 21. Ex. 1005 at 8:3-27, 14:30-15:5. Accordingly, the lower electrodes are located on the exposed upper surface of the topmost insulating layer circuit substrate 100 in these connection windows 12a (here, insulating layer 8), as shown by Figure 2 of Childs, above, and therefore are located on the surface of the "transistor array substrate" required by claim 1.

179. Further, I note that while lower electrode 21 is on top of the same insulating layer 8 upon which aluminum electrodes 3 and 4 are formed in the OLED

structure depicted in Fig. 2 of Childs, a POSA during the timeframe of the '338 patent would have found it obvious (and been motivated) to instead form lower electrode 21 on the surface of a different insulating layer that covers those aluminum electrodes 3 and 4. In particular, a POSA would have considered two routine and straightforward ways of making such a modification to Childs.

180. A first option for making the modification I have described above would have been, after forming aluminum electrodes 3 and 4, to form an additional transparent insulating layer on top of those electrodes, *then* to form lower electrode 21 on the top of that new transparent insulating layer. A second option for making that modification would have been to form lower electrode not on insulating layer 8, but instead on planar insulating layer 12 (this second option would have simply required reordering the manufacturing steps of Childs).

181. Regarding the first option for the modification proposed above, I note that a number of other contemporary prior art references disclosed forming the anode electrodes for each pixel directly on an insulating layer that covers the transistor array, such as a planarization layer. As I have explained above, Kobayashi disclosed forming its "first electrodes" 117 directly on the "insulating layer 116" that serves as a planarization film, Ex. 1003 at ¶ [0074], as illustrated by Figure 7 of Kobayashi:

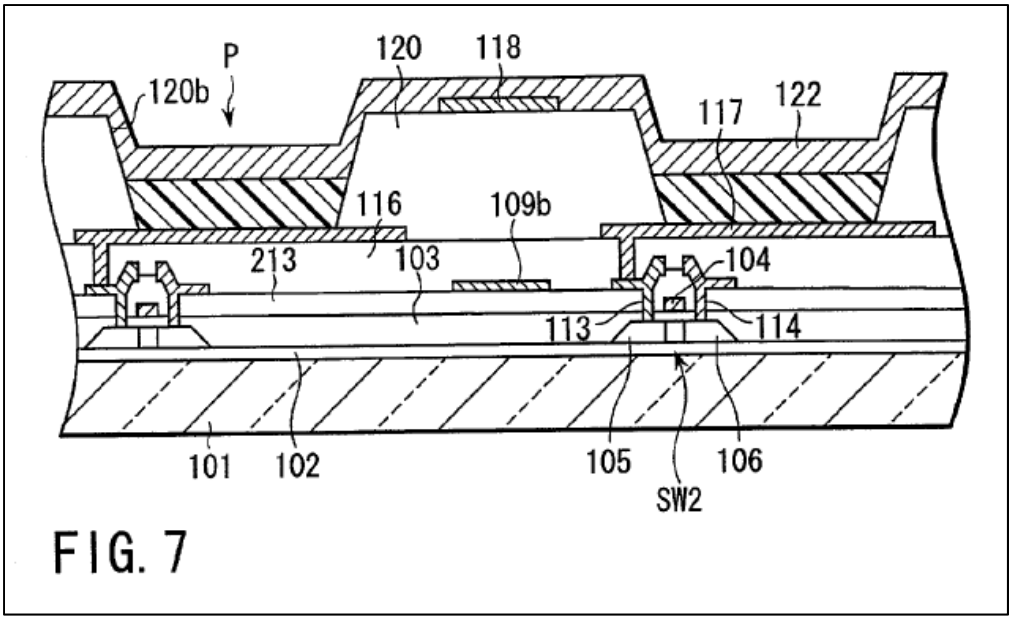
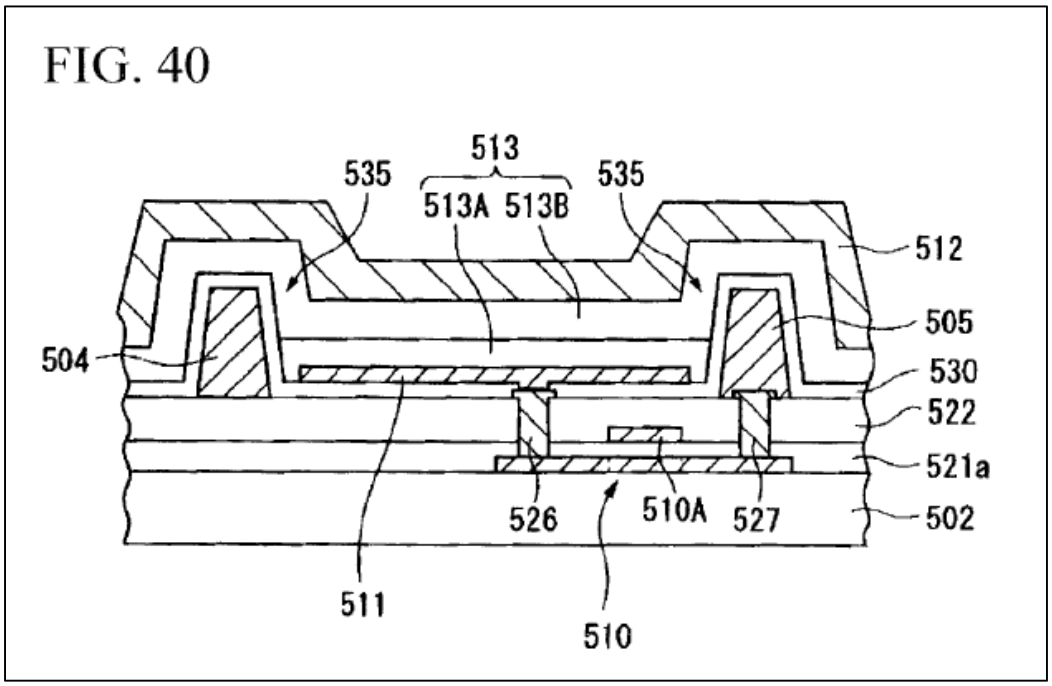
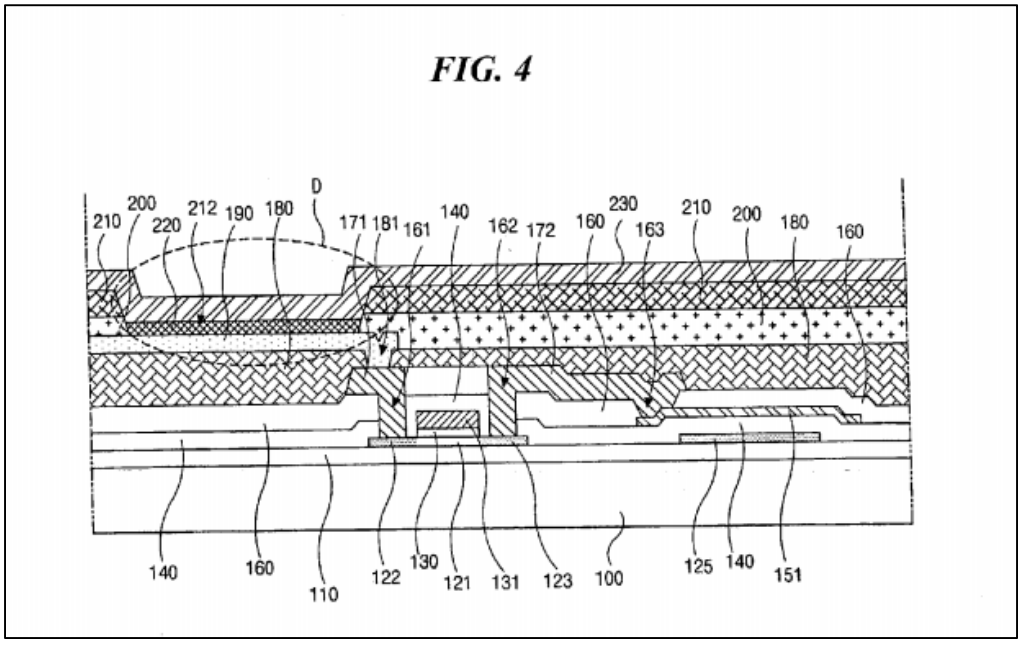


FIG. 7

182. Similarly, Nakamura disclosed forming a transparent ITO "pixel electrode 511" on top of "inter-layer insulating layer 522," and then connecting that pixel electrode 511 to the transistor array via "contact hole 523," Ex. 1009 at ¶¶ [-[0182], [0326]-[0328], as depicted in Fig. 40 of Nakamura:



183. Another such OLED structure was demonstrated by Park, in which "passivation layer 180" with "a planar upper surface" is formed to cover metal "drain electrode 171 and source electrode 172" before "[a] first electrode 190 made of a transparent conductive material" (ITO, Ex. 1014 at ¶ [0046) is "disposed on the planar upper surface of the passivation layer 180," Ex. 1014 at ¶ [0036], as illustrated by Figure 4 of Park:



184. Other prior art references from the time period of the '338 patent explained why a POSA would have been motivated to create a separate, insulating planarization layer on top of the metal transistor electrodes, and then to form the pixel electrodes on top of that additional insulating planarization layer. U.S. Patent Application Publication No. 2002/0000576 ("Inukai") (Ex. 1016), for example, disclosed that forming an "interlaying insulating film" on top of the thin-film

transistor array of an OLED would create "a good, level surface" for forming the OLED elements on top of that level insulating film, and that this was important because the OLED elements themselves could be "extremely sensitive to unevenness." Ex. 1016 at ¶¶ [0310]-[0311]. This is illustrated by Fig. 14 of Inukai, which depicts "pixel electrode 849" formed on level "interlayer insulating film 848" above the TFTs 8201, 8202, 8203, and 8204:

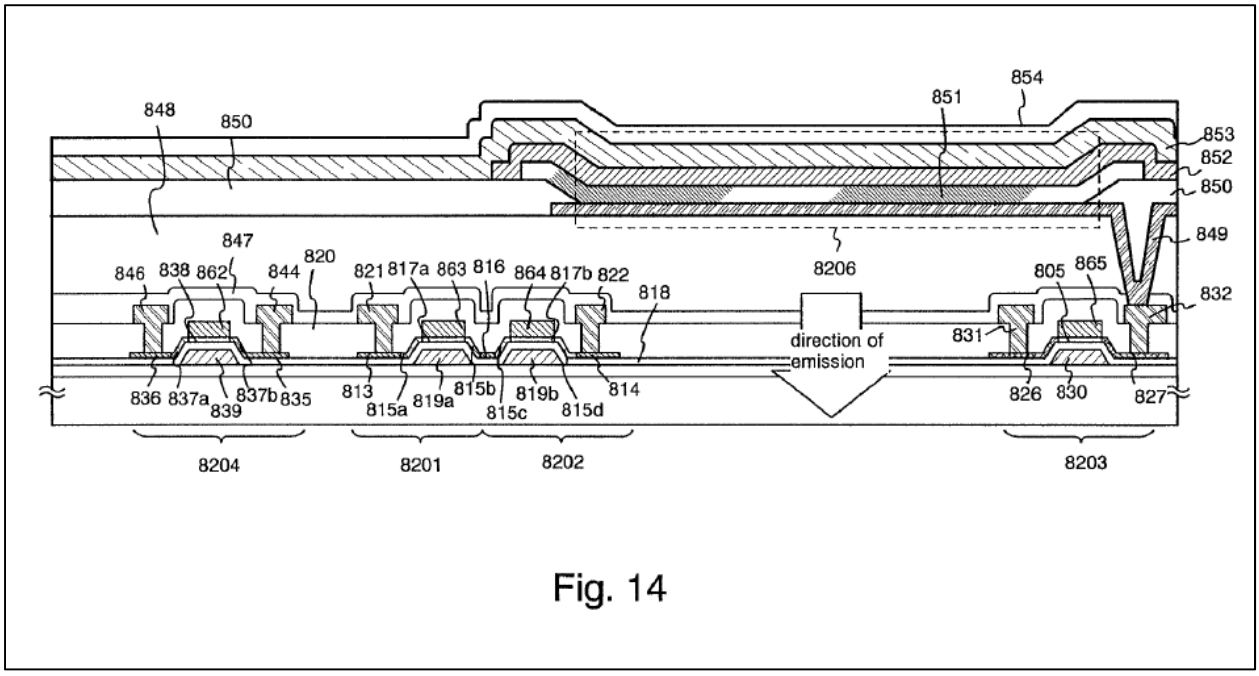
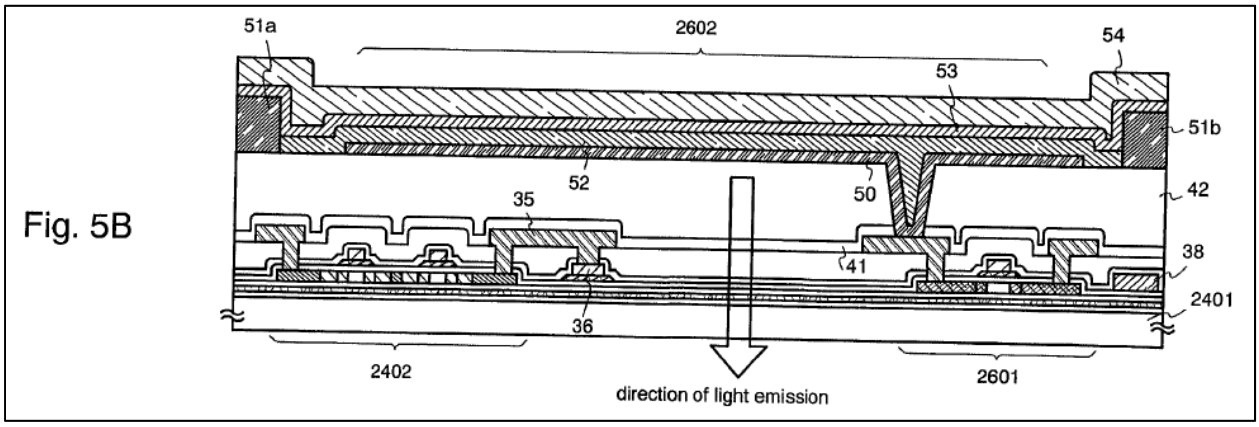


Fig. 14

185. Another prior art reference that discussed the motivation for adding such a separate insulating planarization layer was U.S. Patent Application Publication No. 2002/0009538 ("Arai") (Ex. 1017). "It is very important" (and "desirable"), Arai stated, to form a level insulating layer on top of the TFT array of an OLED structure "before forming the pixel electrode so that the light-emitting layer can be formed on as flat [of a] surface as possible," Ex. 1017 at ¶ [0077], as

illustrated by Fig. 5B of Arai, which shows "pixel electrode 43" being formed on "leveling film" 42:

Fig. 5B



186. Making either of the modifications discussed above (adding another transparent insulating layer under lower electrode 21, or forming lower electrode 21 on planar insulating layer 12) would also have been a straightforward change for a POSA, which would have required little more than a standard change to the photomasks used to fabricate the TFT array of Childs, in order to create "windows" through that additional insulating layer (or the planar insulating layer) so as to connect that underlying TFT array to the OLED elements. I note that such windows 12b already exist in Childs' planar insulating layer 12 in order to connect the conductive barriers 240 to the transistor array elements within circuit substrate 100. And Childs' specification already explains that "[c]onnection windows (such as vias 12a, 12b, 12x, etc.) are opened in the layer 12 in known manner, for example by photolithographic masking and etching." Ex. 1005 at 14:29-15:2. Childs also repeatedly states that "photolithographic masking and etching techniques" such as

this were already "known" to those of skill in the art by the September 2004 timeframe. Ex. 1005 at 15:25-28, 16:8-10.

187. Additionally, forming the lower electrodes 21 of Childs on Childs' planar insulating layer 12 would have required ensuring that the planar insulating layer 12 was transparent, so that light emitted by the OLED elements could be transmitted through the transparent lower electrodes 21 as well as through the planar insulating layer 12. But a POSA would have recognized that this was disclosed by Childs as well—Childs discloses that the "planar insulating layer 12" can be made "for example of silicon nitride," Ex. 1005 at 8:24-27, and then repeatedly states that transparent "silicon dioxide" can be used as an alternative "insulating material" to silicon nitride. Ex. 1005 at 15:24-28, 16:21-24. Accordingly, a POSA would have recognized that forming the "planar insulating layer 12" out of transparent silicon dioxide would allow light emitted by the OLED elements to pass through planar insulating layer 12 when the pixel anode electrodes 21 were formed on the surface of that planar insulating layer 12.

188. Further, in my opinion, making either of these obvious design choices would, in fact, have actually worked to simplify the manufacturing process for Childs' OLED structure. The design illustrated in Fig. 2 of Childs would have required extra steps to manufacture layers 3, 4, and 12, because the deposition, patterning, and etch of the "metal electrodes "3 and 4," which Childs discloses are

made "typically of aluminum," Ex. 1005 at 8:3-8, needs to be followed by the formation of the lower electrodes 21, which Childs discloses are formed from "indium tin oxide (ITO)," Ex. 1005 at 8:19-22.

189. The formation of these aluminum metal electrodes 3 and 4 must be performed by vacuum deposition so as to prevent oxygen contamination. Oxygen contamination would result in the creation of aluminum oxide, and while aluminum is a good electrical conductor, aluminum oxide is an insulator. In contrast to this oxygen-free manufacturing process for the aluminum electrodes 3 and 4, the formation of the indium tin oxide electrodes 21 requires some oxygen in the deposition process, in order to mix with the indium and tin to create the indium tin oxide transparent conducting material.

190. Therefore, the processing of these two different types of conductive elements (the aluminum metal electrodes 3 and 4 vs. the indium tin oxide electrode 21) would require great care in order to prevent oxidation of the aluminum electrodes during the formation of the indium tin oxide electrodes. A common and straightforward way to prevent oxidation of the aluminum electrodes would have been to use a protective insulating layer over the aluminum during the formation of the indium tin oxide electrodes in order to prevent oxidation of those aluminum electrodes.

191. More specifically, in the Childs patent, the lower electrodes 21 will require additional physical vapor deposition of indium tin with oxidation, patterning, and etch to form the ITO lower electrodes 21, while at the same time preventing any additional etching or oxidation of the aluminum metal electrodes 3 and 4 during the formation of those ITO lower electrodes 21. By forming an additional insulating layer over electrodes 3 and 4 before forming lower electrodes 21 (or by forming the lower electrodes 21 on the planar insulating layer 12), the additional insulating layer underneath the lower electrodes 21 will itself provide the required oxygen protection to the aluminum metal electrodes 3 and 4 from any additional etching or oxygen contamination during the formation and processing of the ITO lower electrodes 21. In summary, opting for this obvious design variant would have simplified the manufacturing process for the layered OLED structure.

192. Finally, I note that a POSA would have recognized that choosing either of the two obvious design variants that I have described above would not have required any changes to the structure of the other OLED elements: for example, because Childs' conductive barriers 240 are so thick, forming the lower electrode 21 on top of planar insulating layer 12 would not have affected those barriers' ability to separate and contain the [electroluminescent] polymer layers 22, Ex. 1005 at 9:3-11, as illustrated by Figure 2 of Childs:

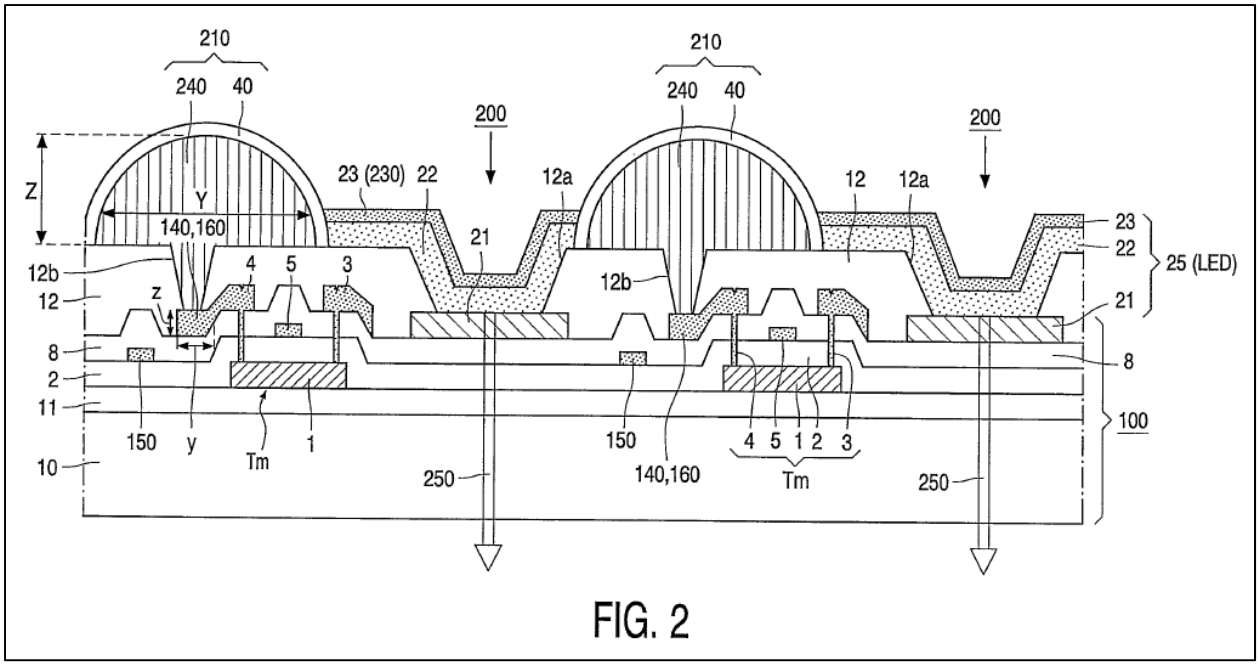


FIG. 2

193. I further note that even if there was a concern about the barriers 210 being significantly thick enough to contain the electroluminescent polymer layers 22 (which, as I have explained above, there is not), a POSA would have recognized that either: a) the barriers could be made thicker (I note that Childs repeatedly notes that the barriers may be "at least" as thick as in the specific examples it provides, Ex. 1005 at 10:25-11:2, and making the barriers thicker would only further decrease the resistance of the electrical component to which conductive barriers 240 are connected); and/or b) a shallower trench/window could be etched in the planar insulating layer 12 and the pixel electrodes 21 could be formed on top of planar insulating layer 12 in that trench/window, using Childs' "known" "photolithographic masking and etching" techniques, Ex. 1005 at 14:29-15:2, 15:25-28, 16:8-10.

1[d]: a plurality of light-emitting layers formed on the pixel electrodes, respectively; and

194. Childs also discloses the claimed "plurality of light-emitting layers." Specifically, Childs discloses that "[e]ach pixel 200 comprises a current-driven electroluminescent display element 25 (21, 22, 23)," Ex. 1005 at 7:10-12, and that "a light-emitting organic semiconductor material 22" is formed "between" each "lower electrode 21 and an upper electrode 23," Ex. 1005 at 8:16-27, as illustrated by Fig. 2:

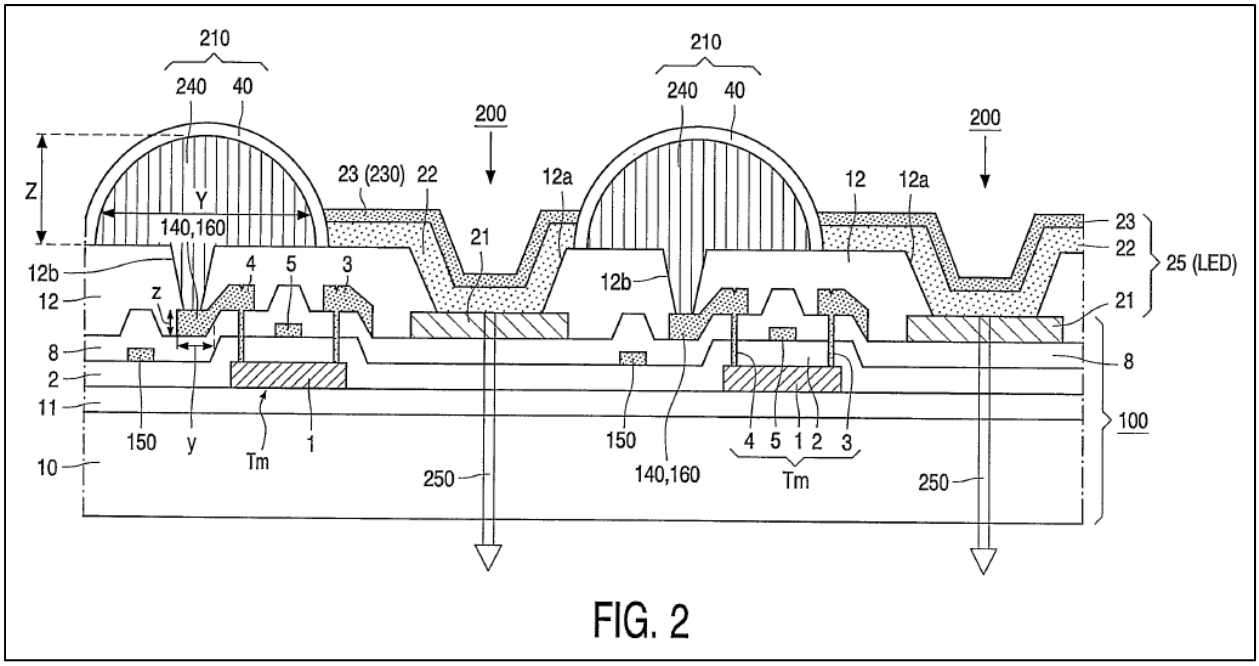


FIG. 2

195. This organic semiconductor material, Childs explains, is used to create "electroluminescent layers 22." Ex. 1005 at 9:3-11, 15:29-31.

196. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

1[e]: a counter electrode which is stacked on the light-emitting layers,

197. Childs discloses the claimed "counter electrode." In particular, as I have explained above, Childs states that "[e]ach pixel 200 comprises a current-driven electroluminescent display element 25 (21, 22, 23)," Ex. 1005 at 7:10-12, and that "a light-emitting organic semiconductor material 22" is formed "between" each "lower electrode 21 and an upper electrode 23," Ex. 1005 at 8:16-27. A POSA would have recognized that this "upper electrode 23," which Childs discloses "may be a cathode," Ex. 1005 at 8:19-22, corresponds to the claimed "counter electrode."

198. Accordingly, a POSA would have appreciated that Childs discloses this limitation.

1[f]: wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

199. A POSA would have recognized that this limitation would have been obvious in view of the combination of Childs and Shirasaki.

200. Childs discloses, for each pixel, a plurality of transistors that include: (a) a driving transistor, one of the source and the drain of which is connected to the pixel electrode, and (b) a switch transistor which makes a write current flow between the drain and the source of the driving transistor.

201. In particular, Childs discloses a "drive TFT T1" which is "connected in series" to the LED element 25. Ex. 1005 at 7:10-30. This corresponds to the claimed "driving transistor, one of which the source and the drain of which is connected to the pixel electrode." Childs also discloses an "addressing TFT T2" which is connected "to the gate of the individual drive TFT T1 of the respective pixel." Ex. 1005 at 7:10-30. This corresponds to the claimed "switching transistor which makes a write current flow between the drain and the source of the driving transistor." These "drive" and "addressing TFTs" are depicted in Figure 1 of Childs:

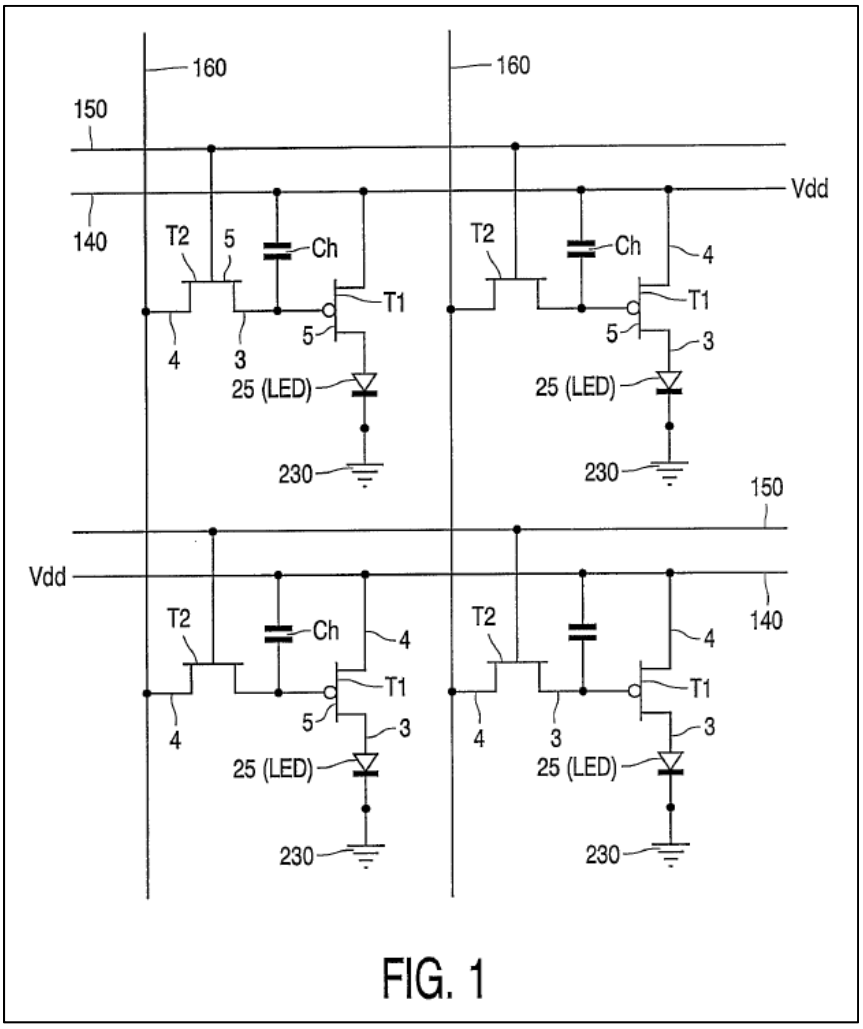


FIG. 1

202. I note, however, that Childs does not disclose a "holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period" as required by Claim 1.

203. The addition of the claimed "holding transistor" to Childs' pixel circuit, however, would have been obvious to a POSA in September 2004, based on Shirasaki, which not only disclosed the exact same three-transistor structure claimed by the '338 patent, but explained why a POSA would have been motivated to replace Childs' two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit.

204. First, regarding the disclosure of Shirasaki, Shirasaki's figures illustrate the same three-transistor pixel circuit that was later used by Casio again in the figures for the '338 patent. I note that transistor 11 in Fig. 5B of Shirasaki corresponds to "switch transistor 21" in Figure 2 of the '338 patent, transistor 12 in Figure 5B of Shirasaki corresponds to "driving transistor" 23 in Figure 2 of the '338 patent, and transistor 10 in Shirasaki corresponds to "holding transistor" 22 in Figure 2 of the '338 patent:

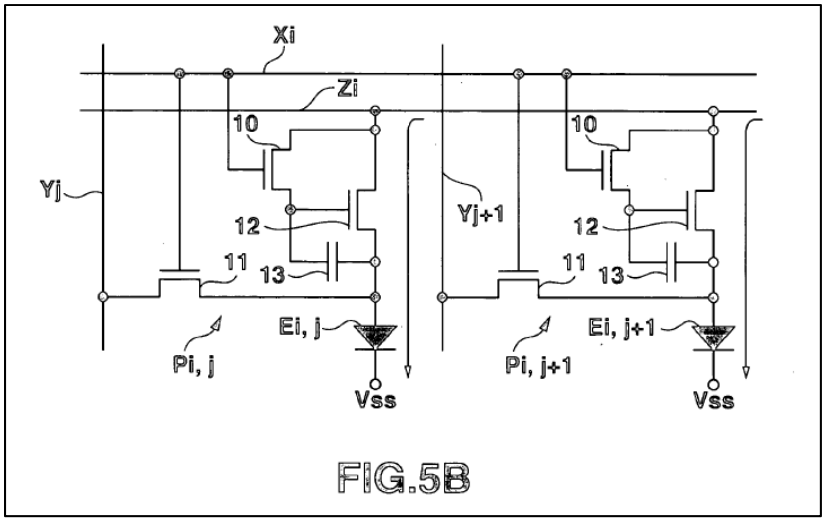


FIG.5B

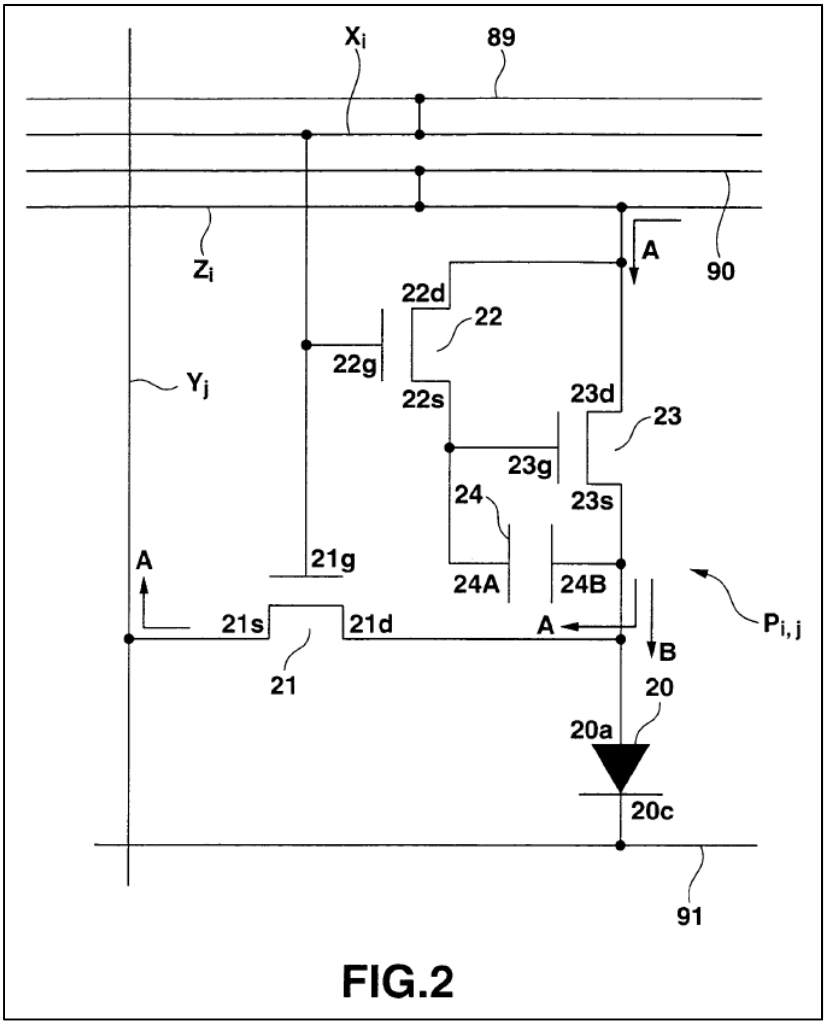


FIG.2

205. Further, as I have explained above, Childs and Shirasaki each disclose AMOLED display panels and the TFT pixel circuits that are found in each pixel of those AMOLED display panels. And as I also note above, Shirasaki not only discloses the three-transistor pixel circuit structure claimed in the '338 patent, but explains why a POSA would have been motivated to replace Childs' two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit.

206. Shirasaki explains that in a "conventional light emitting element display," where "two transistors are formed in one pixel," Ex. 1004 at ¶¶ [0003], [0004], that:

> The channel resistances of the transistors 103 and 104 depend upon the ambient temperature and change after a long-term operation. Therefore, it is difficult to display images with a desired luminance tone for long time periods.
>
> . . .
>
> This varies the magnitudes of the drain-source currents of the transistors 104 in the individual pixels, resulting in variations in the display characteristics of the individual pixels in a single panel. As a consequence, no accurate tone control can be performed. Accordingly, variations in the characteristics of the transistor 104 of each pixel must fall within a range required to control the tone of each pixel. However, as the resolution of an EL element increases, it becomes more difficult to make the characteristics of the transistors 104 of the individual pixels uniform.
>
> Ex. 1004 at ¶ [0007].

207. Shirasaki goes on to explain the multiple benefits that result when that two-transistor pixel circuit structure are replaced with its disclosed three-transistor pixel circuit structure:

> In the display panel having the above [three-transistor] arrangement, the current memory circuit stores the current data corresponding to the current value of the memory current flowing during the selection period. Accordingly, the display current having a current value substantially equal to the memory current can be supplied to the optical element. Current control is thus performed by the current values, not by voltage values. This suppresses the influence of variations in the voltage-current characteristic of the control system and allows the optical element to stably display images with desired luminance.
>
> Ex. 1004 at ¶ [0018].

208. Shirasaki also specifically states that "one advantage of the present invention is that pixels stably display image with desired luminance in a display panel." Ex. 1004 at ¶ [0011]. I note that while Childs discloses "a holding capacitor Ch" (shown above) that "hold[s] the resulting conductive state of the drive TFT T1," Ex. 1005 at 7:23-39, a POSA would have recognized that this capacitor would not have provided the same advantages as Shirasaki's "holding transistor"—as evidenced by the fact that the pixel circuits of both Shirasaki as well as of the '338 patent still include a capacitor in addition to the claimed "driving," "switch," and "holding" transistors in their pixel circuits.

209. Furthermore, Shirasaki explains why a three-transistor structure should be chosen instead of a pixel circuit with four or more transistors per pixel, Ex. 1004 at ¶ [0009], stating that in its three-transistor pixel circuit structure "the display area per pixel of a display panel is increased" and therefore "the apparent brightness improves accordingly" (in comparison to a four-transistor (or more) pixel circuit structure), Ex. 1004 at ¶¶ [0012], [0020]. Shirasaki also explains that the three-transistor circuit will have a comparatively "low voltage and consequently low power consumption driving." Ex. 1004 at ¶ [0019].

210. Accordingly, a POSA would have recognized the advantages provided by Shirasaki's three-transistor pixel circuit structure, and would have been motivated to modify Childs' AMOLED display panel by replacing its two-transistor pixel circuit with the three-transistor pixel circuit disclosed by Shirasaki.

211. Furthermore, it would have been straightforward for a POSA to modify Childs in the manner I have described above, and a POSA would have readily expected success in (and predictable results from) making this modification for several different reasons.

212. First, as I have discussed above, Shirasaki discloses that its three-transistor pixel circuit was designed and meant to replace the two-transistor pixel circuits found in "conventional" AMOLED devices such as Childs, Ex. 1004 at ¶¶ [0002]-[0008], [0013]-[0019], and thus a POSA would have readily expected

success in modifying Childs in this manner. This expectation of success would have been further bolstered by the fact that both Childs and Shirasaki are directed to AMOLED display panels with thin-film transistor circuits. Ex. 1005 at 1:5-7, Ex. 1004 at ¶¶ [0041], [0043].

213. Further, as I have explained at length above, Childs explains how all of the thin-film transistors that make up its pixel circuits (and the wiring of that "circuitry") are contained within "circuit substrate 100" underneath the "planar insulating layer 12" "that extends over the thin-film structure of the substrate 11." Ex. 1005 at 7:31-8:15, 8:24-27.

214. Accordingly, a POSA would have recognized that Childs' two-transistor pixel circuit could be replaced with Shirasaki's three-transistor pixel circuit without altering the layer structure of any of the layers above Childs' "circuit substrate 100" (which, as I have discussed above, corresponds to the claimed "transistor array substrate"). I note that Childs itself states that:

> Other pixel circuit configurations are known for active matrix display devices, and it should be readily understood that the present invention may be applied to the pixel barriers of such a device regardless of the specific pixel circuit configuration of the device.
>
> Ex. 1005 at 7:6-9.

215. Further, while modifying Childs to replace its two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit would have necessitated

changing the photomasks used to fabricate the TFT array in Childs and relocating the "windows" through Childs' "planar insulating layer 12," these were known and routine manufacturing steps to a POSA at the time that would have been involved during the fabrication of any AMOLED device. Childs notes this as well, repeatedly describing how "photolithographic masking and etching techniques" such as this were already "known" to those of skill in the art by the September 2004 timeframe. Ex. 1005 at 14:29-15:2, 15:25-28, 16:8-10.

b. Dependent Claim 2

> **A panel according to claim 1, wherein said plurality of interconnections include at least one of a feed interconnection connected to the other of the source and the drain of at least one of the driving transistors, a select interconnection which selects at least one of the switch transistors, and a common interconnection connected to the counter electrode.**

216. In my opinion, based on the language of this claim and the disclosure of the '338 patent, a POSA would have understood this claim to require that the claimed plurality of interconnections include at least one of the three types of interconnections described in the claim ("feed," "select," or "common") (as opposed to requiring at least one of each of the three types of interconnections, as claim 4 requires).

217. Further, a POSA would have appreciated that Childs discloses this claim limitation. Childs explains that its plurality of interconnections include one or more feed interconnections connected to the other of the source and the drain of at

least one of the driving transistors. Specifically, Childs discloses that the "conductive barrier[s] 240" are "connected to and/or from one or more circuit elements" such as "supply line 140," Ex. 1005 at 9:20-29, which is connected to the drive TFT T1, Ex. 1005 at 7:10-17, as shown in Figure 1 of Childs:

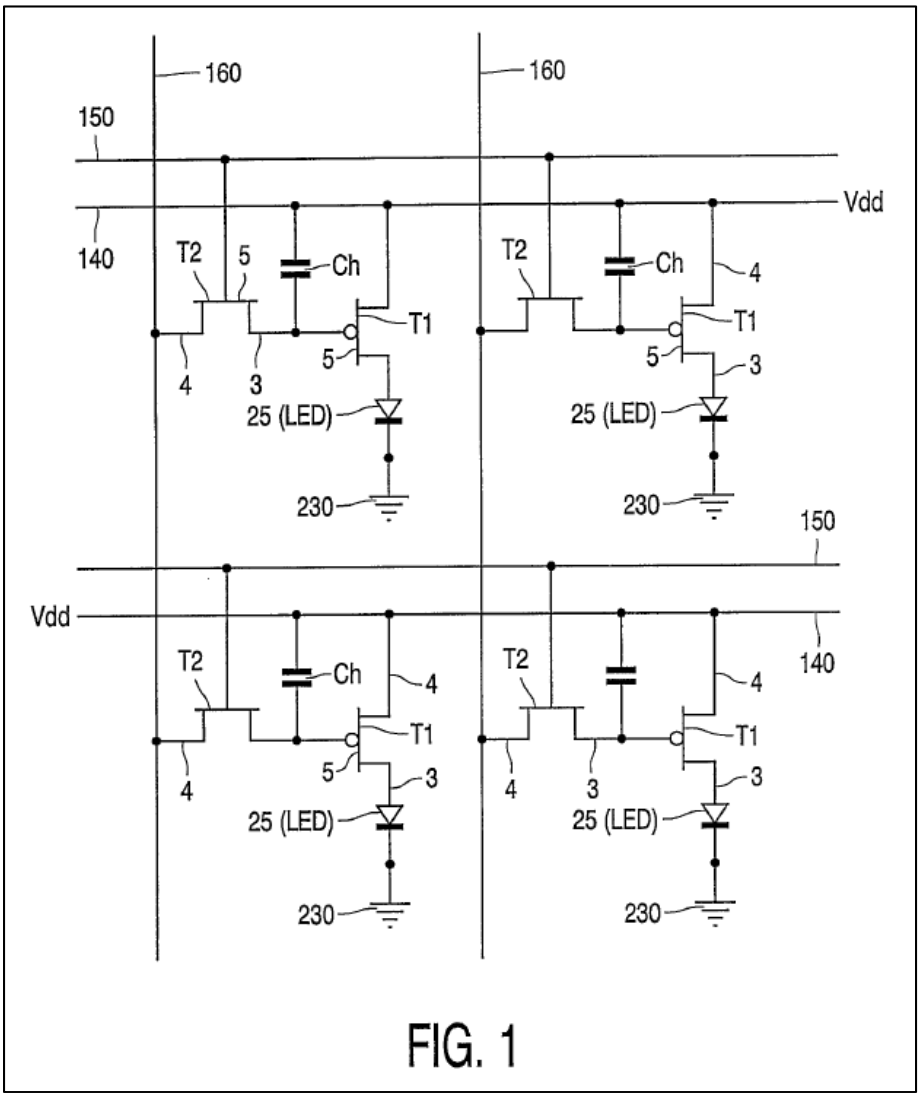


FIG. 1

218. Additionally, Childs further discloses that its plurality of interconnections include one or more select interconnections which selects at least one of the switch transistors. Childs teaches that its "conductive barrier[s] 240," in

addition to supplementing the voltage supply lines 140, also supplement "addressing line 150," Ex. 1005 at 9:20-29, which serve to carry the "selection signal" that "turns on the addressing TFT T2," Ex. 1005 at 7:18-22, as shown in Figure 1 above.

219. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

c. Dependent Claim 3

A panel according to claim 2, wherein each of the light-emitting layers is formed between two of the feed interconnection, the select interconnection, and the common interconnection.

220. A POSA would have appreciated that Childs discloses this claim limitation. As depicted in Figure 1, Childs' pixels 200 are each bordered on one side by addressing line 150, and on the other side by voltage supply line 140:

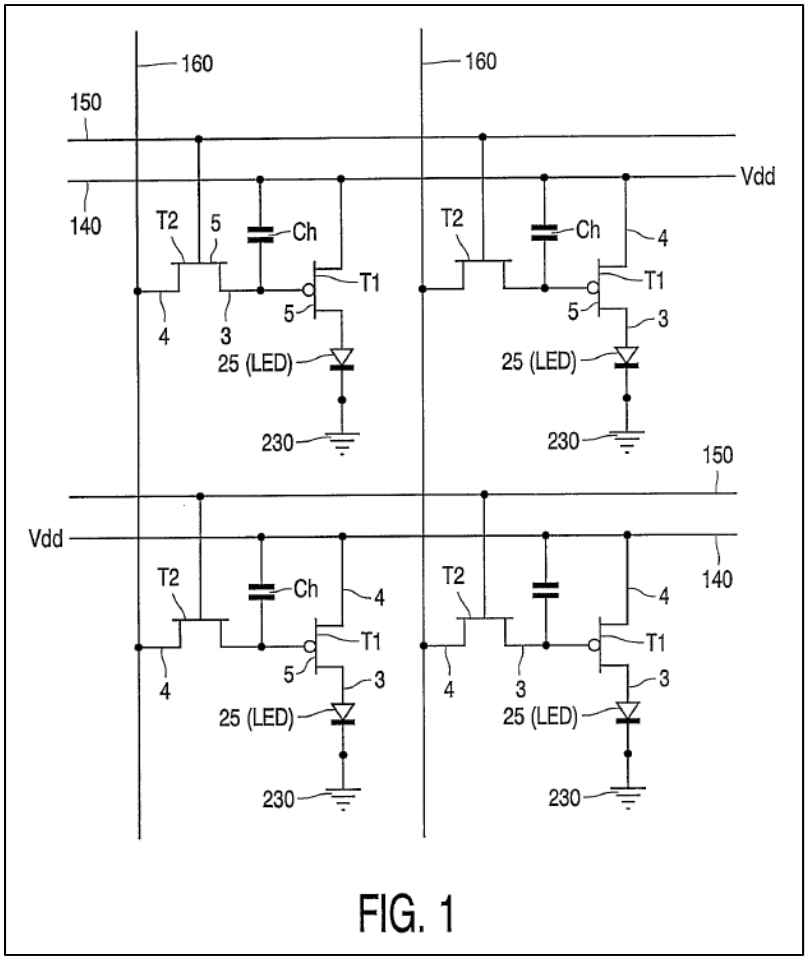


FIG. 1

221. In particular, Childs discloses a first "metal core 240" of a first "barrier 210" that "form[s] (or back[s] up)" "addressing line 150," (corresponding to the claimed select interconnection) in addition to a second "metal core 240x" of a second "barrier 210x" that "form[s] (or back[s] up)" "supply line 140" (corresponding to the claimed feed interconnection). Ex. 1005 at 11:11-21. This is illustrated by Figures 5 and 6 of Childs, depicting the pixels 200 (which, as I have explained above, each contain organic light-emitting layers) being formed between these projecting interconnections 210 (on the top of the pixel) and 210x (on the bottom of each pixel)

(I note that there appears to be an inadvertent typographical error, as the metal core 240x in barrier 210x is mistakenly labeled "240"):

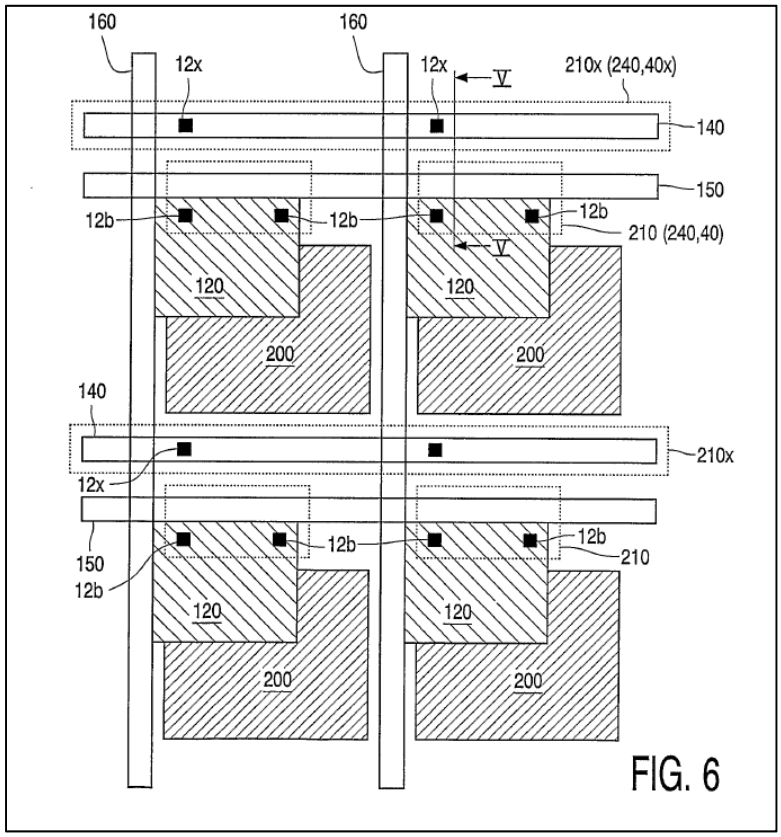


FIG. 6

222. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

d. Dependent Claim 5

A panel according to claim 1, wherein said plurality of pixels include a red pixel, a green pixel, and a blue pixel.

223. A POSA would have appreciated that Childs disclosed that the plurality of pixels include a red pixel, and green pixel, and a blue pixel. Childs itself discloses that its barriers "prevent pixel overflow of conjugate polymer materials that may be ink-jet printed for red, green and blue pixels of a color display." Ex. 1005 at 1:20-

2:1. Furthermore, it would have been well-known to a POSA in the September 2004 timeframe of the '338 patent that a color OLED display would include red, green, and blue pixels. For example, as I have discussed above, Kobayashi explained that a color OLED panel "comprises three kinds of display elements P, which respectively emit red, green, and blue light." Ex. 1003 at ¶ [0041]. Nakamura (Ex. 1007 at Fig. 33A) similarly disclosed this teaching.

224. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

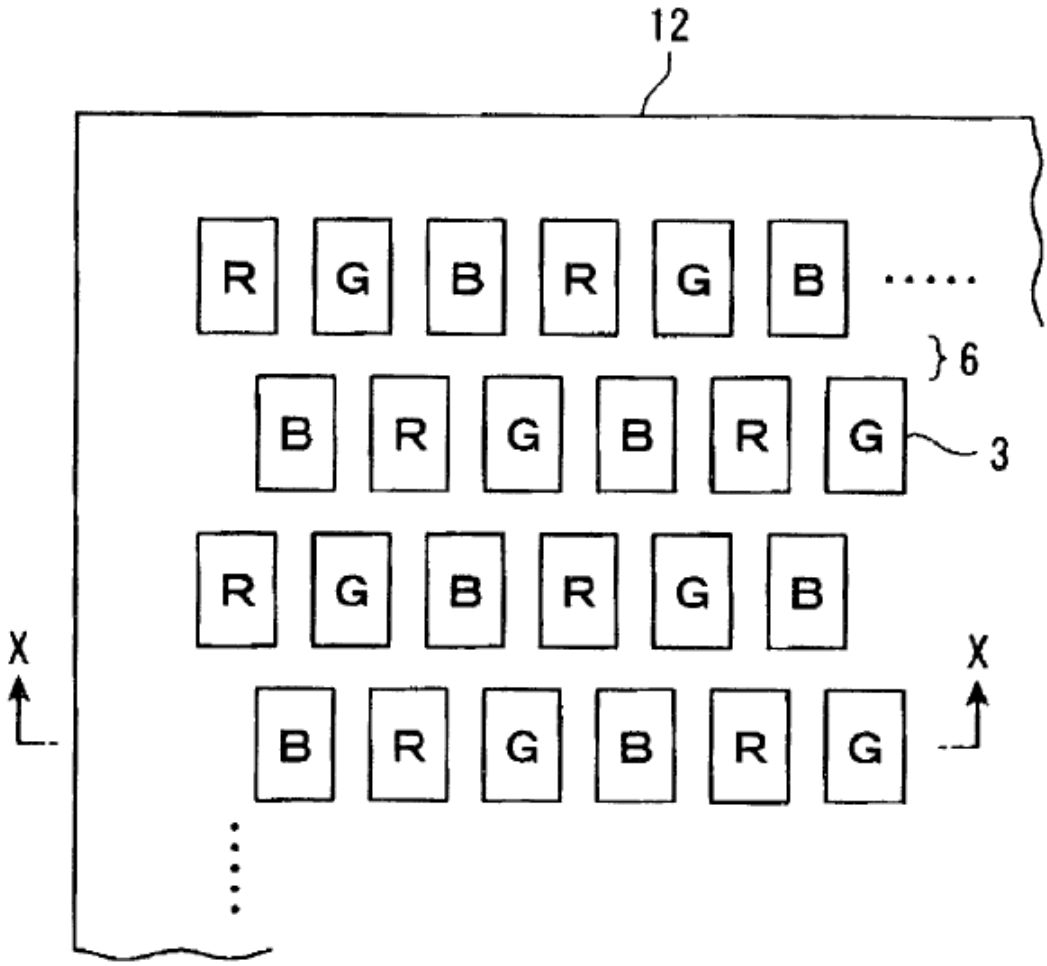
e. Dependent Claim 6

A panel according to claim 5, wherein said plurality of pixels comprises a plurality of sets each including the red pixel, the green pixel, and the blue pixel arrayed in an arbitrary order.

225. A POSA also would have appreciated that Childs disclosed that the plurality of pixels comprises a plurality of sets each including the red pixel, the green, pixel, and the blue pixel arrayed in an arbitrary order. As I have noted above, Childs discloses that its barriers "prevent pixel overflow of conjugate polymer materials that may be ink-jet printed for red, green and blue pixels of a color display." Ex. 1005 at 1:20-2:1. Furthermore, a POSA would have recognized that these red, green, and blue pixels would be arrayed in an arbitrary order. Such RGB displays were well known to those of skill in the AMOLED art at the time, and contemporary prior art such as Nakamura, for example, commonly disclosed that

such displays would be arranged in an arbitrary order, as illustrated by Figure 33A of Nakamura (Ex. 1007):

FIG. 33A



226. Accordingly, a POSA would have appreciated that Childs disclosed this claim limitation.

f. Dependent Claim 7

"A panel according to claim 1, wherein at least one of the interconnections has a thickness of 1.31 to 6.00 μm."

227. Childs discloses that its interconnections have a thickness falling within this claimed range. Specifically, Childs states that its "conductive barrier material" (corresponding to the claimed interconnections, as discussed above) "may have a thickness Z," and in the only specific example that Childs provides for that thickness, states that "Z may be between 2 μm and 5 μm" (within the claimed range). Ex. 1005 at 10:30-11:2.

g. Dependent Claim 8

A panel according to any one of claims 1 or 2 to 7, wherein at least one of the interconnections has a width of 7.45 to 44.00 μm.

228. Childs discloses that its interconnections have a width falling within this claimed range. Specifically, Childs states that its "conductive barrier material" (corresponding to the claimed interconnections, as discussed above) "may have a line width Y," and in the only specific example that Childs provides for that width, states that "Y may be 20μm" (within the claimed range). Ex. 1005 at 11:3-6.

h. Dependent Claim 9

A panel according to claim 1, wherein at least one of the interconnections has a resistivity of 2.1 to 9.6 μΩcm.

229. Childs discloses that its interconnections have a width falling within this claimed range. As noted by Kobayashi, the resistivity of the interconnections

depends on the particular "conductive material" used to construct them (as opposed to the geometry and/or dimensions of those interconnections, which would determine their resistance). Ex. 1003 at ¶ [0049], Fig. 4. And Childs states that it is preferable to use "aluminium or copper" for the "electrically conductive material 240" used to form Childs' interconnections. Ex. 1005 at 10:6-10, 16:27-28. This corresponds to the materials cited by the '338 patent itself as falling within this claimed resistivity range, as the '338 patent discloses that interconnections will have a "resistivity of 2.1 to 9.6 μΩcm" "when an Al-based or Cu is used" to construct those interconnections. Ex. 1001 at 21:58-62.

230. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

i. Dependent Claim 10

A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer that is different from a layer forming the source and the drain of each of the transistors and a layer forming the gate of the transistors.

231. Childs discloses that its "conductive metal barriers 240" (which, as I have explained above, correspond to the claimed "plurality of interconnections") are formed from a conductive layer that is different from the layer 1 forming the source and the drain of each of the transistors, and the layer 5 forming the gate of each of the transistors. Ex. 1005 at 8:3-15, 10:6-10. This is illustrated by Figure 2 of Childs:

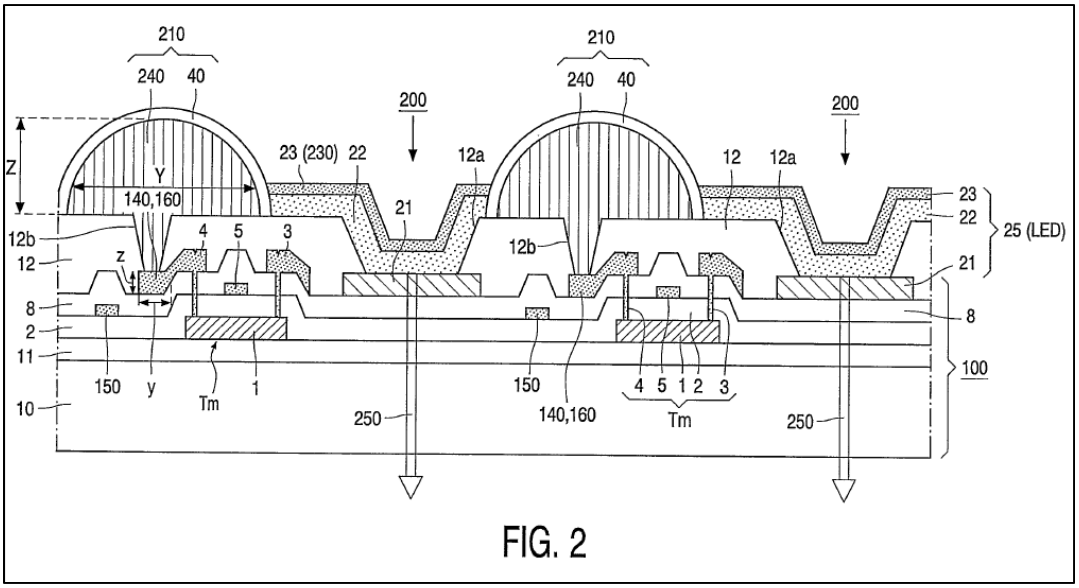


FIG. 2

232. Furthermore, Childs discloses that while the source and drain regions 1 are made from polysilicon and the gate electrode 5 is made from aluminum or polysilicon, Ex. 1005 at 8:3-8, the conductive metal barriers 240 are instead made from metal with "very low resistivity," such as "aluminum or copper or nickel or silver," Ex. 1005 at 10:6-8, and would therefore need to be formed in a different layer.

233. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

j. Dependent Claim 11

A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer different from a layer forming the pixel electrodes.

234. Childs discloses that its "conductive metal barriers 240" (which, as I have explained above, correspond to the claimed "plurality of interconnections") are

also formed from a layer different from the layer forming the pixel electrodes. This is illustrated by Figure 2 of Childs:

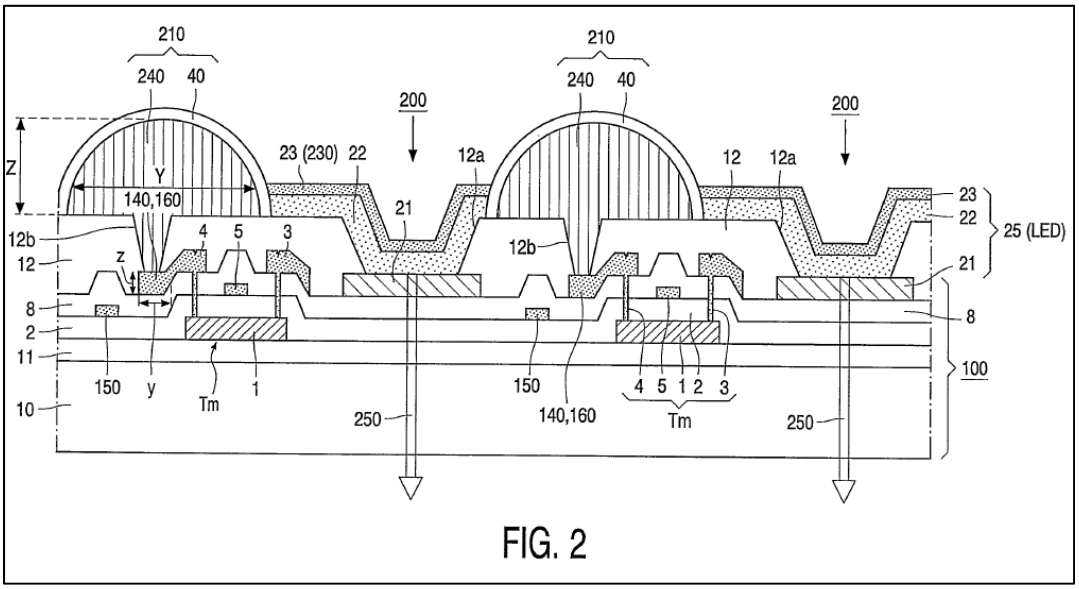


FIG. 2

235. Further, Childs discloses that each of its lower electrodes 21 (which, as explained above, correspond to the claimed pixel electrodes) "may be an anode of indium tin oxide (ITO)," Ex. 1005 at 8:19-22, in contrast to the conductive metal barriers 240, which are made from metal with "very low resistivity," such as "aluminum or copper or nickel or silver," Ex. 1005 at 10:6-8, and would therefore need to be formed in a different layer.

236. Accordingly, a POSA would have appreciated that Childs discloses this claim limitation.

k. Dependent Claim 12

A panel according to claim 1, wherein said plurality of interconnections are thicker than a layer forming the source and the

drain of each of the transistors and a layer forming the gate of each of the transistors.

237. Childs discloses that its "conductive metal barriers 240" (which, as I have explained above, correspond to the claimed "plurality of interconnections") are thicker than the layers forming the source, drain, and gate of each of its transistors. Childs discloses that its conductive barrier material 240 "may have a thickness Z that is a factor of two or more (for example at least five times) larger than the thickness z of this conductor layer 5(150)," which forms the gate of each of the transistors "in the circuit substrate 100." Ex. 1005 at 10:30-11:1.

238. Figure 2 of Childs further illustrates how the conductive metal barriers 240 are substantially thicker than each of layer 1 (which forms the source and drain of the transistors) and layer 5 (which forms the gate of each of the transistors):

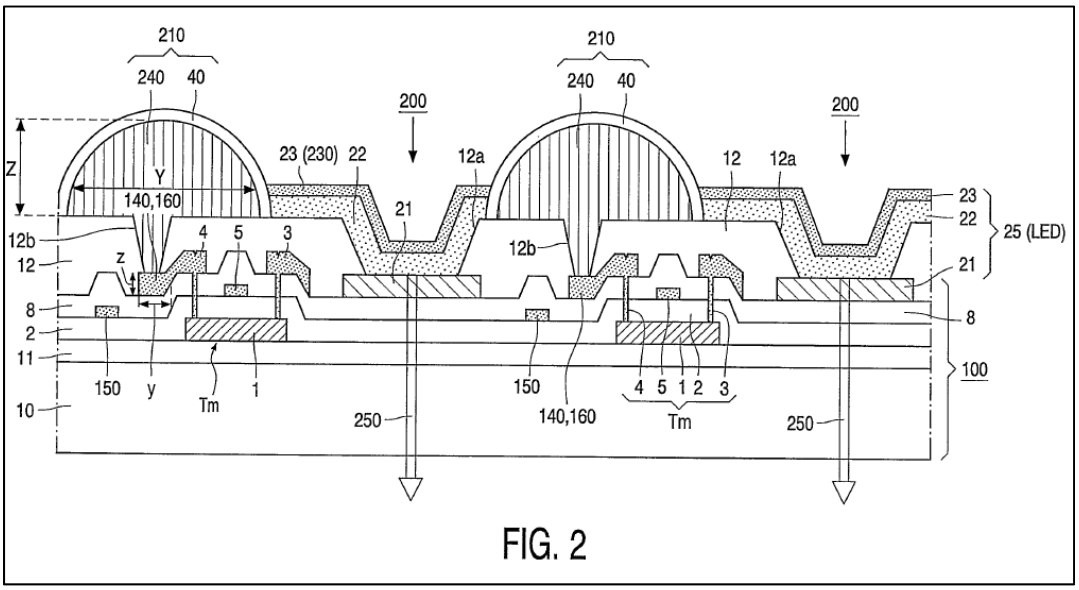


FIG. 2

l. Dependent Claim 13

A panel according to claim 1, wherein said plurality of interconnections are thicker than the pixel electrodes.

239. Childs discloses that its "conductive metal barriers 240" (which, as I have explained above, correspond to the claimed "plurality of interconnections") are thicker than the pixel electrodes. Childs discloses that its conductive barrier material 240 "may have a thickness Z that is a factor of two or more (for example at least five times) larger than the thickness z of this conductor layer 5(150)," Ex. 1005 at 10:30-11:1, while the "lower electrode 21" (corresponding to the claimed pixel electrode) "is formed as a thin film," Ex. 1005 at 8:22-24.

240. Figure 2 of Childs further illustrates how the conductive metal barriers 240 are substantially thicker than layer 21 (which forms the pixel electrodes of Childs' OLED pixels 200):

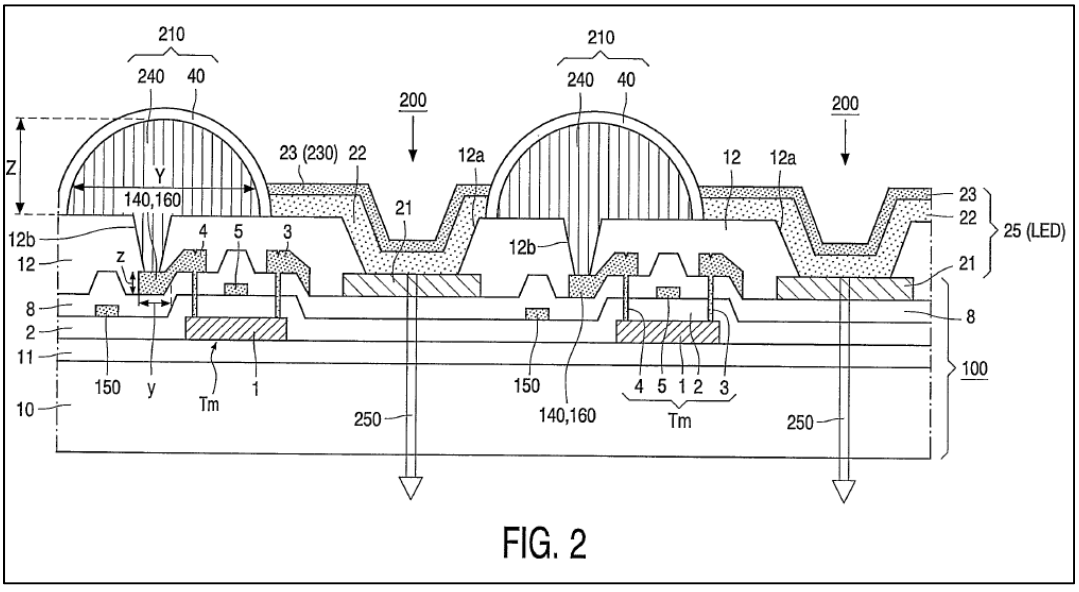


FIG. 2

* * *

241. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

December 18, 2019
Date

Adam Fontecchio, Ph.D.